



Hi EFFICIENT

WIDE-BANDGAP TECHNOLOGIES FOR TOMORROW'S HIGHLY EFFICIENT
AND RELIABLE AUTOMOTIVE MOBILITY SOLUTIONS

**“A new frontier in GaN power technology: GaN System-on-Chips
for power electronic applications”**

Herbert De Pauw (imec)

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ChipsJU



Outline

- Introduction
- GaN base line technology 100V and 650V
- GaN System-on-Chip features
 - GaN power HEMTs in HB configuration
 - Integrated gate driver with/without levelshifters
 - PWM generator
 - 4-terminal or 2-terminal temperature sensors
 - 1% current-sense terminals
- GaN System-on-Chip realisations and measurements

Introduction

- IMEC
 - world-leading innovation hub in nano-electronics and digital technologies
 - headquarters in Leuven (Belgium)
 - > 12000m² cleanroom capacity
 - > 5,500 skilled people – over 95 nationalities
 - driving advances in microchip technology

⇒ www.imec.be



Introduction

- GaN at IMEC
 - 20 engineers + operators
 - 3 dedicated teams
 - Epitaxy
 - Integration
 - Device
 - 15+ years of experience
 - 200mm fab
 - Transition to 300mm fab
 - 3000 GaN-wafers grown per year



Introduction

- Why GaN ?
 - bench marks for power switches
 - On-state \Rightarrow resistance as low as possible
 - Off-state \Rightarrow block high-voltage with low leakage current
 - trade-off between on-state and off-state

$$R_{ON} = \frac{4 \cdot V_{BD}^2}{\epsilon_S \cdot \mu_n \cdot E_C^3}$$

B. J. Baliga, 'Fundamentals of power semiconductor devices,' Springer, 2008.

	$\epsilon_S \cdot \mu_n \cdot E_C^3$
Si	1
4H-SiC	207
h-GaN	1191
Diamond	4267

Introduction

- Why GaN System-on-Chip (GaN SoC) ?
 - size reduction
 - single chip solution vs multiple chip solutions
 - exploit the GaN power HEMT to its maximum
 - by monolithic integration of the gate driver
 - reduced parasitics (R,L and C)
 - increased switching frequency
 - smaller passives
 - by introducing extra functionality
 - over- and under-voltage protection
 - gate signal generation
 - dead-time control
 - ...

Introduction

- GaN SoC applications in  **Hi EFFICIENT**

powertrain inverters



UC2

on-board charger



UC5

vehicle solar panel converter

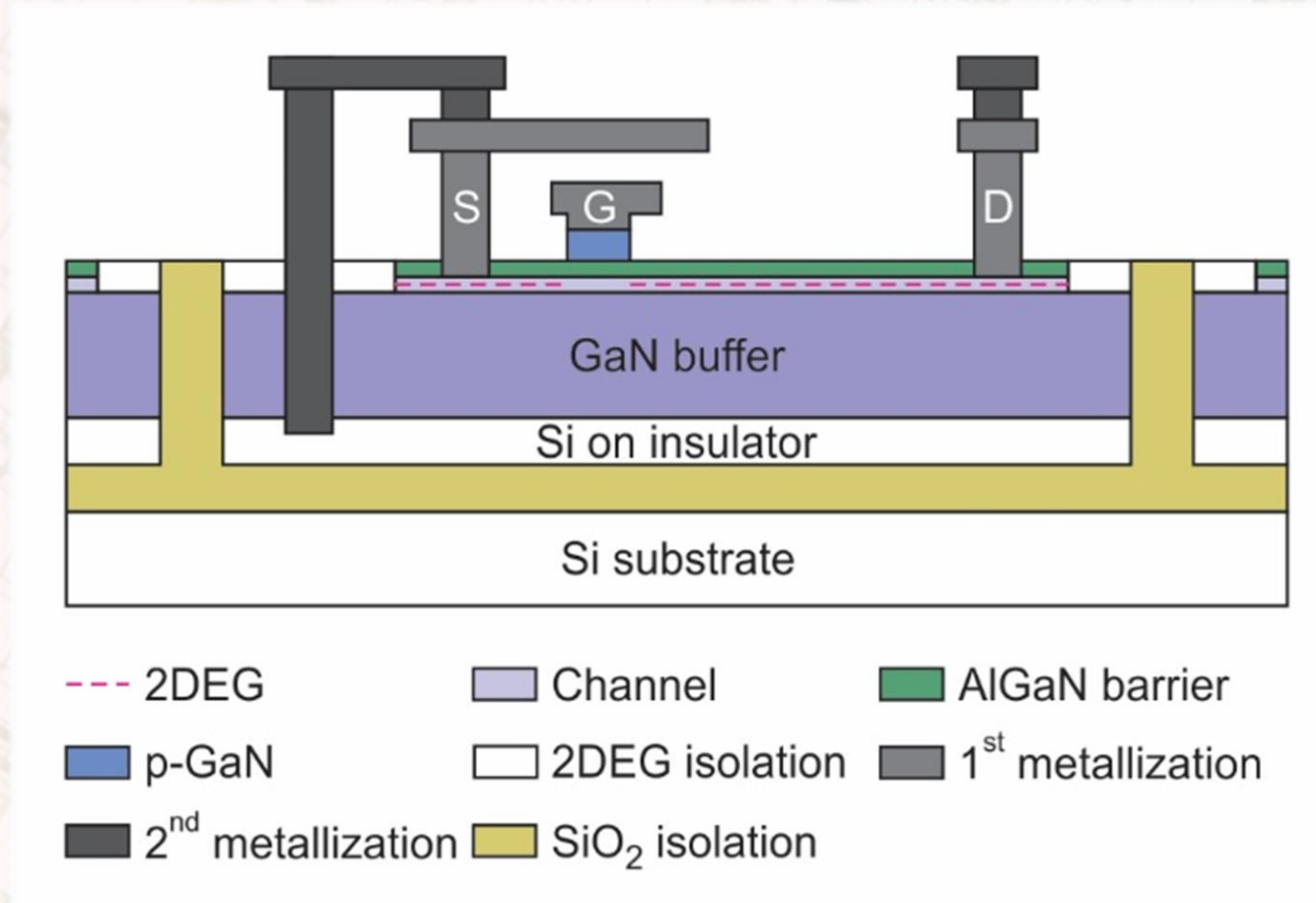


UC6

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GaN base line technology for 100V and 650V



GaN base line technology for 100V and 650V

- Available devices
 - HV power HEMT
 - $V_{\text{threshold}} = 2.5\text{V}$
 - LV HEMT
 - $V_{\text{threshold}} = 2.5\text{V}$
 - high-ohmic / low-ohmic resistor
 - capacitors

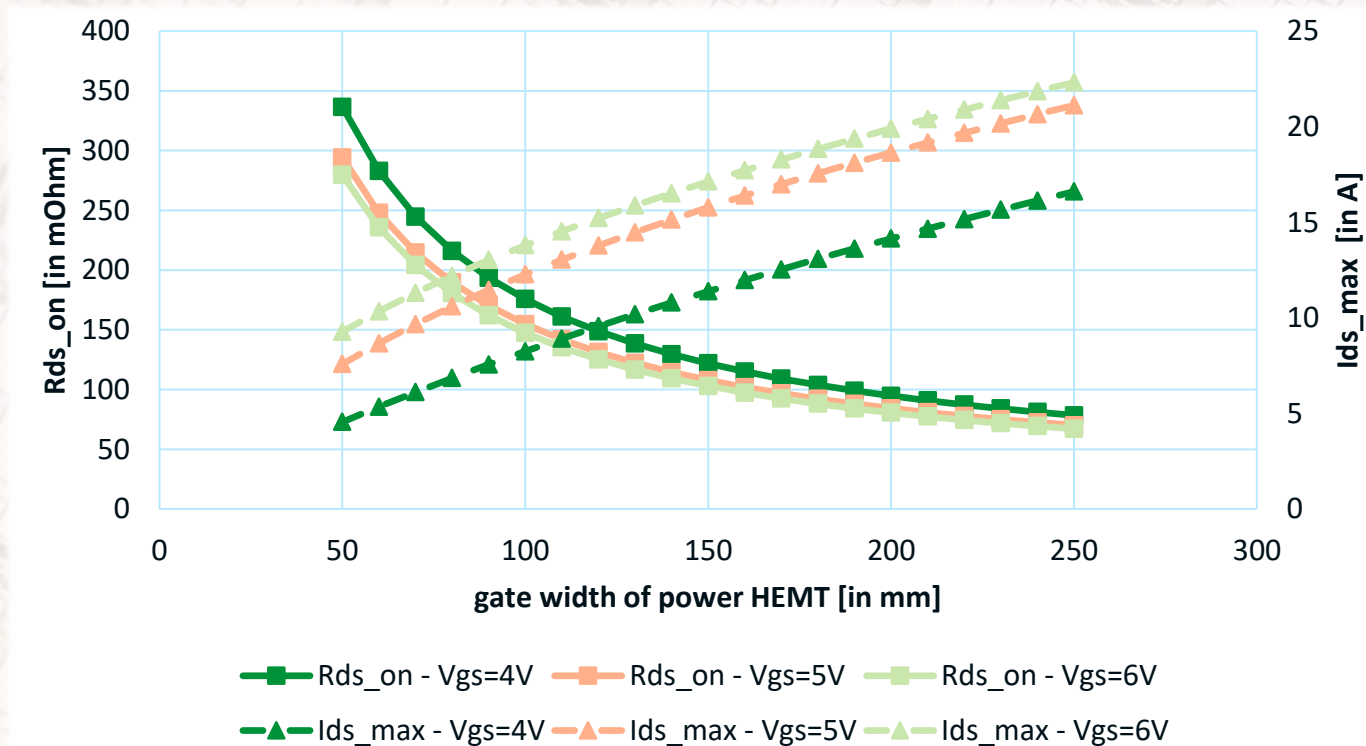
⇒ resistor-transistor logic circuits / analog circuits

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GaN System-on-Chips features

- GaN power HEMT
 - R_{ds_on} / I_{ds_max} versus V_{gs} variation



GaN System-on-Chips features

- GaN power HEMT

100V SoCs

Gate width	Rds_on	Ids_max
1000mm	8.5mΩ	125A
750mm	10mΩ	100A
500mm	15mΩ	70A
160mm	45mΩ	25A

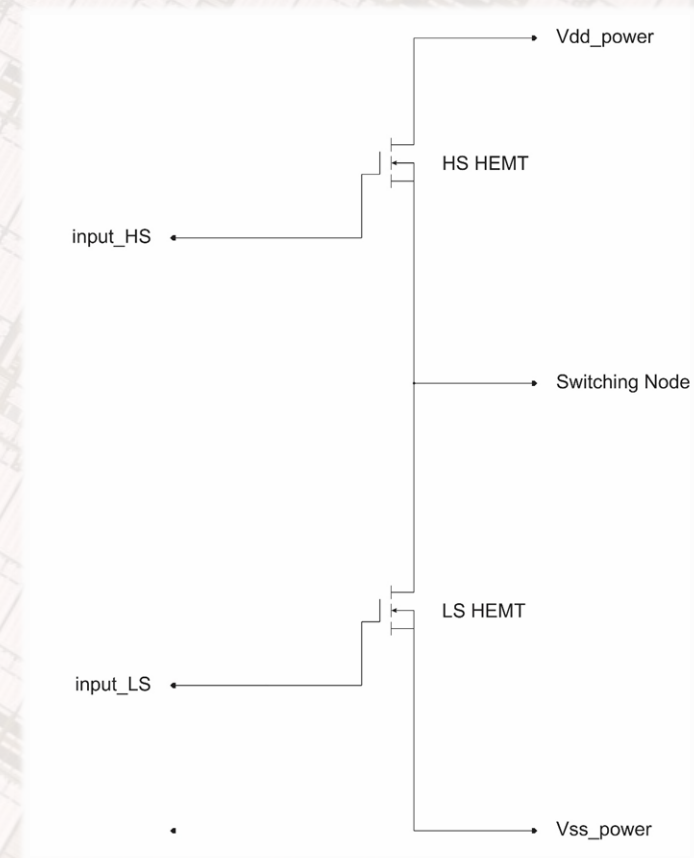
650V SoCs

Gate width	Rds_on	Ids_max
157mm	105mΩ	16A
140mm	115mΩ	15A
125mm	130mΩ	14A
117mm	135mΩ	13A
50mm	300mΩ	7A

Rds_on conditions: Vgs=5V, Vds=1V, temperature=25°C
Ids_max conditions: Vgs=5V, temperature=25°C

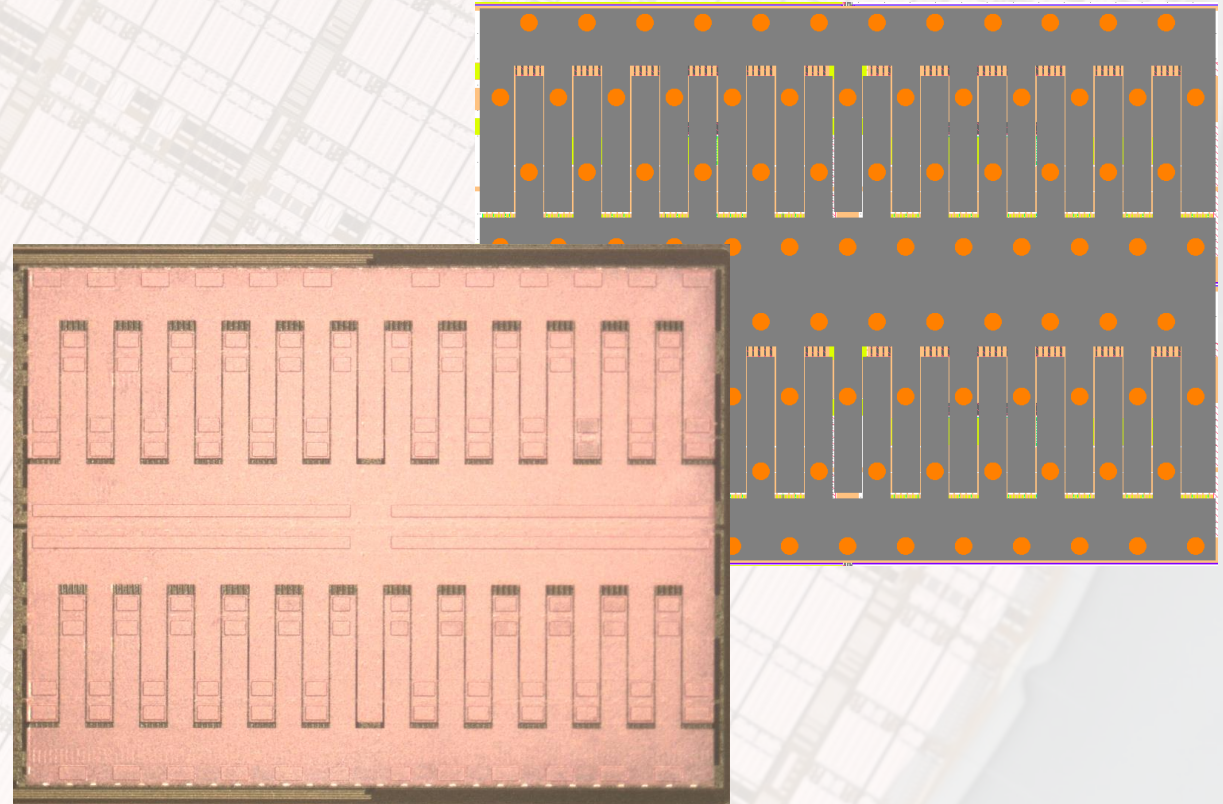
GaN System-on-Chips features

- GaN power HEMTs in HB configuration
 - 2 power HEMTs in series
 - LS HEMT and HS HEMT
 - in separate HV pockets
 - 2 LV terminals
 - 3 HV terminals
 - symmetrical or asymmetrical



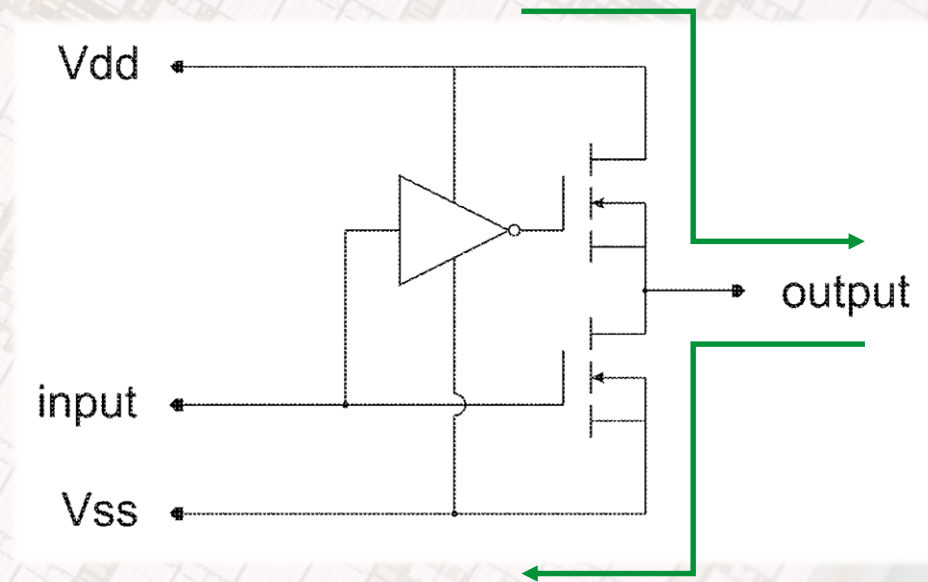
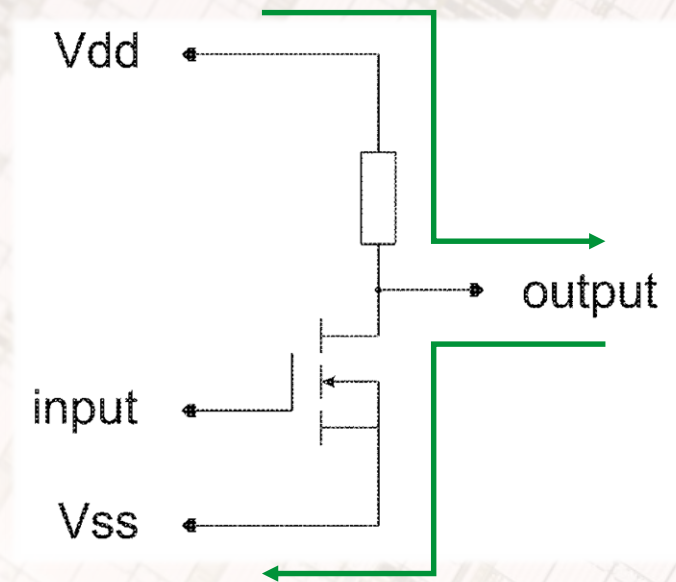
GaN System-on-Chips features

- GaN power HEMTs in Half-Bridge (HB) configuration
 - Largest part in SoCs
 - 1000mm HB in 100V
 - 157mm HB in 650V
 - Layout
 - top metal Cu = grey color
 - connections = orange circles
 - area distributed



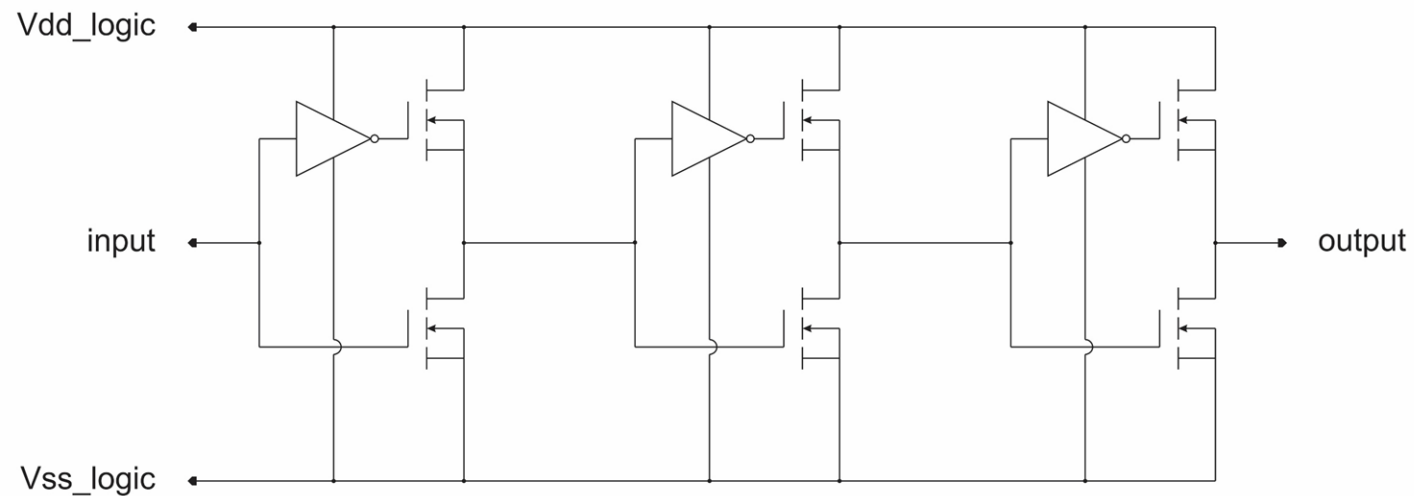
GaN System-on-Chips features

- Integrated gate driver
 - 'inverter' vs 'push-pull' implementation



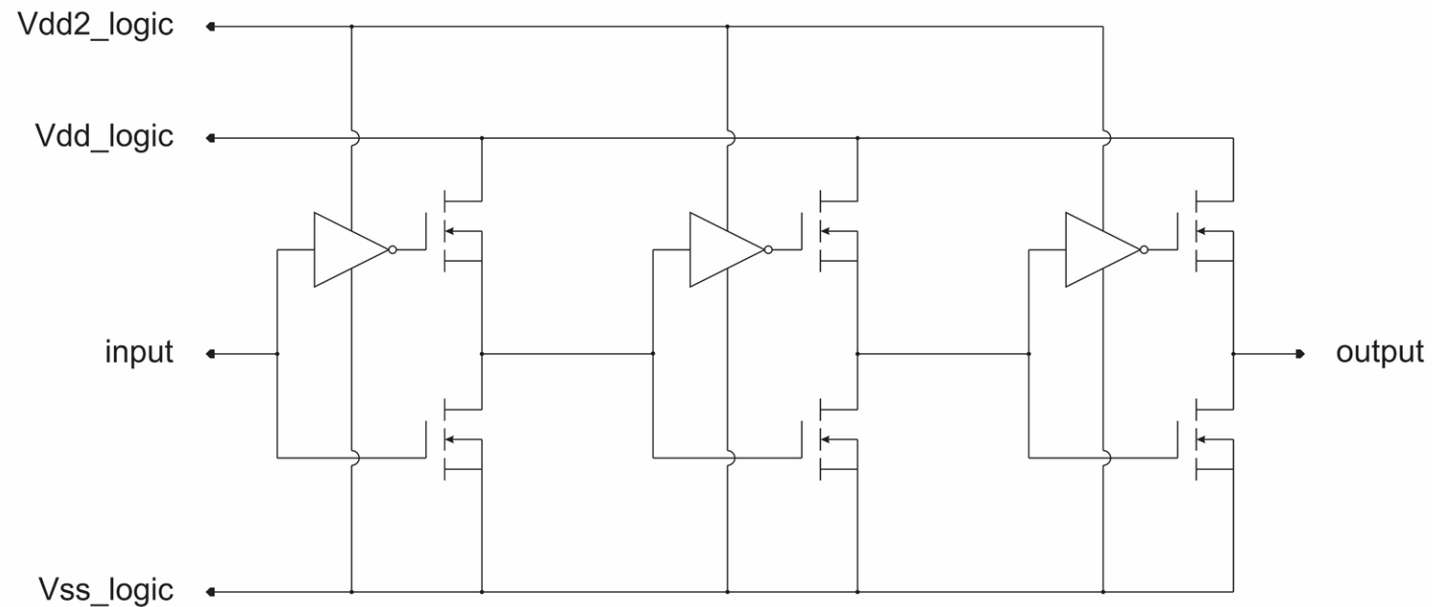
GaN System-on-Chips features

- Integrated gate driver
 - single-supply push-pull version



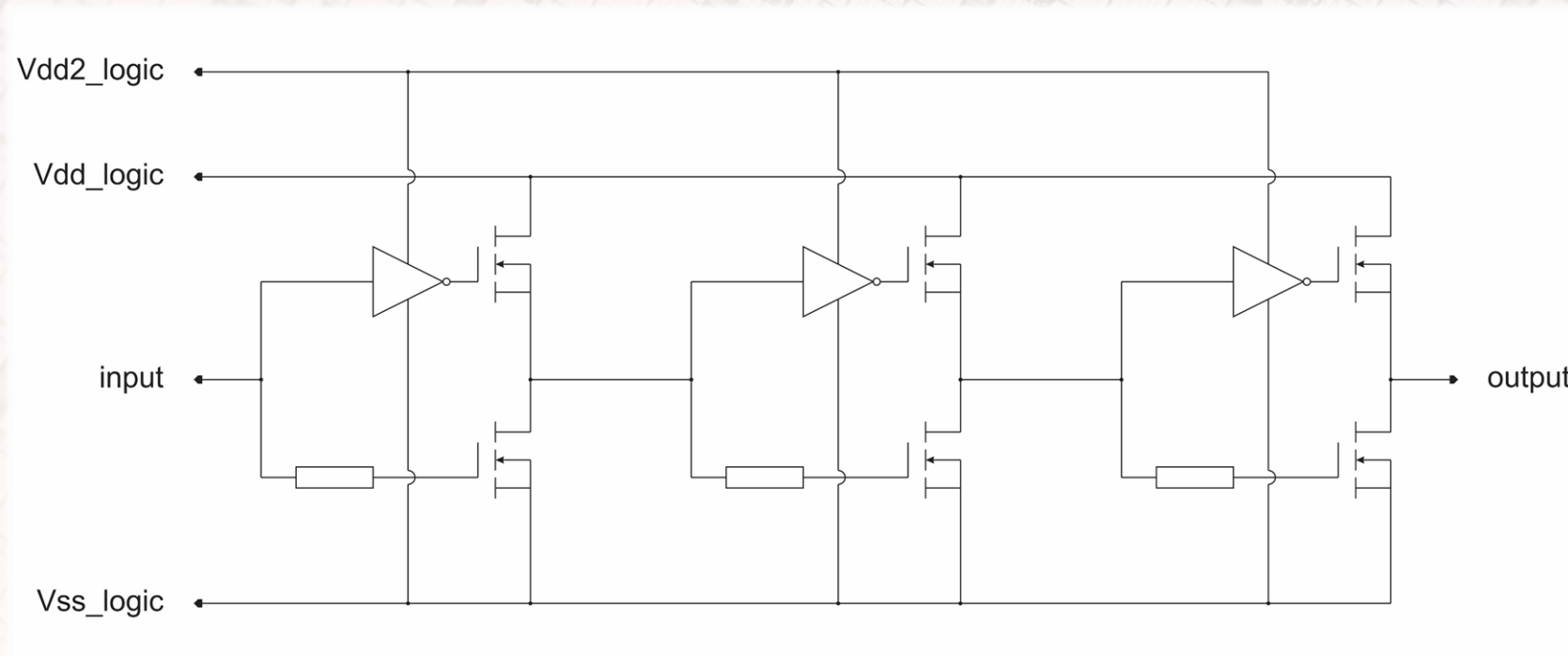
GaN System-on-Chips features

- Integrated gate driver
 - dual-supply push-pull version



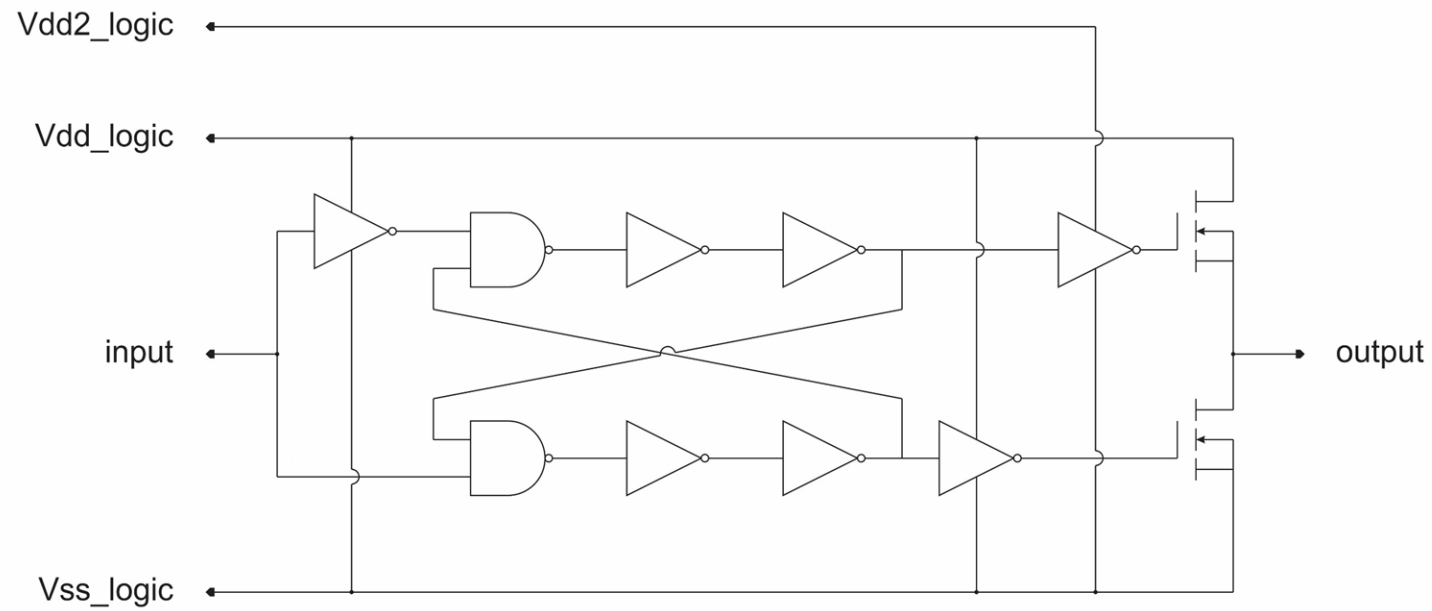
GaN System-on-Chips features

- Integrated gate driver
 - dual-supply push-pull version with 'delay' resistors



GaN System-on-Chips features

- Integrated gate driver
 - cross-coupled NAND port version

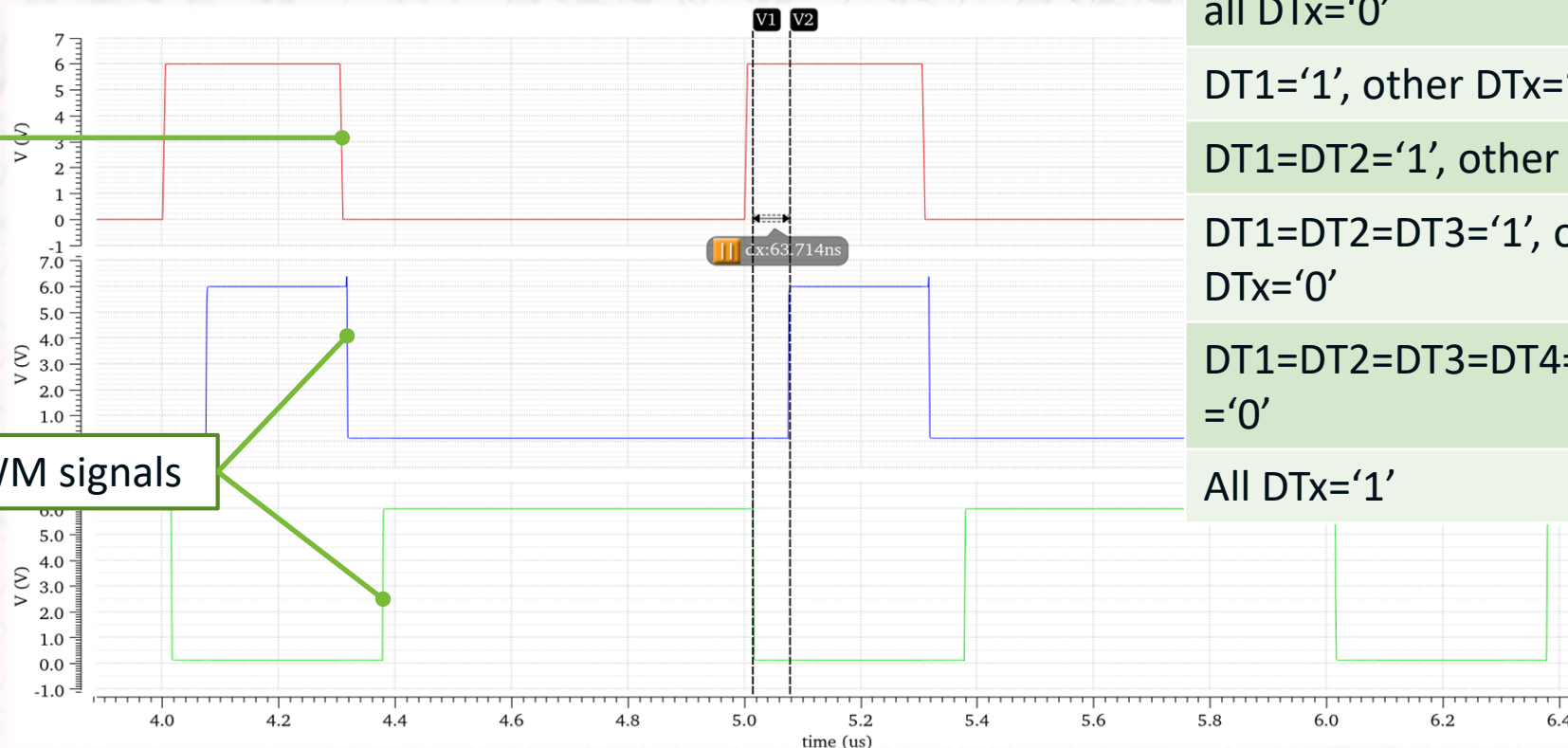


GaN System-on-Chips features

- PWM generator

dead-time control inputs	dead time
all DTx='0'	24ns
DT1='1', other DTx='0'	33ns
DT1=DT2='1', other DTx='0'	42ns
DT1=DT2=DT3='1', other DTx='0'	50ns
DT1=DT2=DT3=DT4='1',DT4='0'	63ns
All DTx='1'	74ns

(valid for 1MHz input)

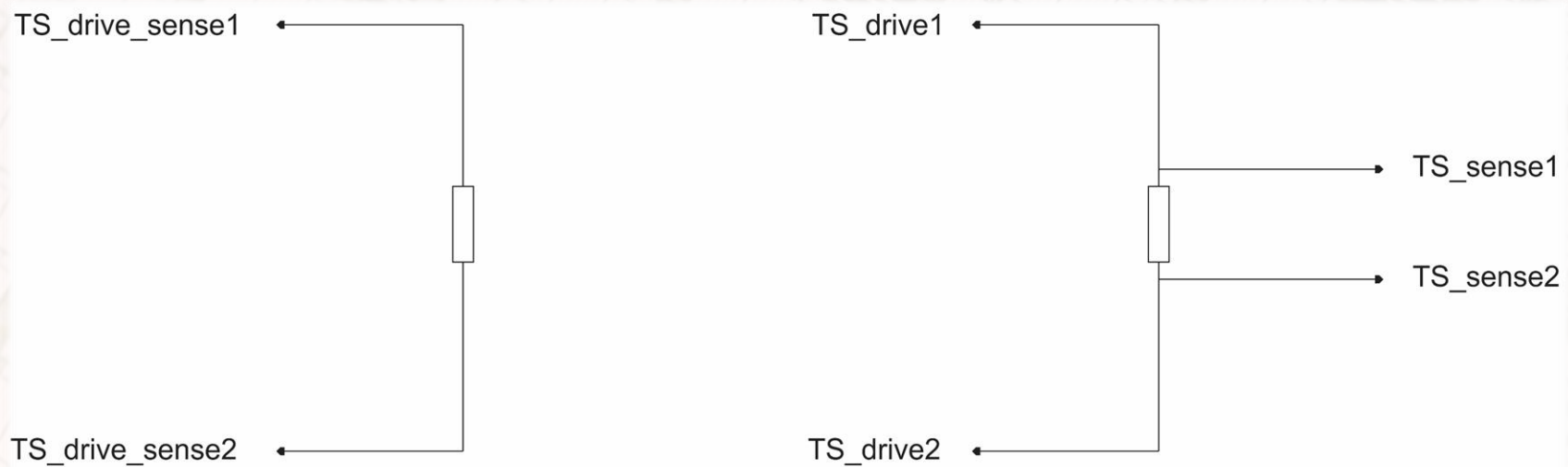


input PWM signal

non-overlapping PWM signals

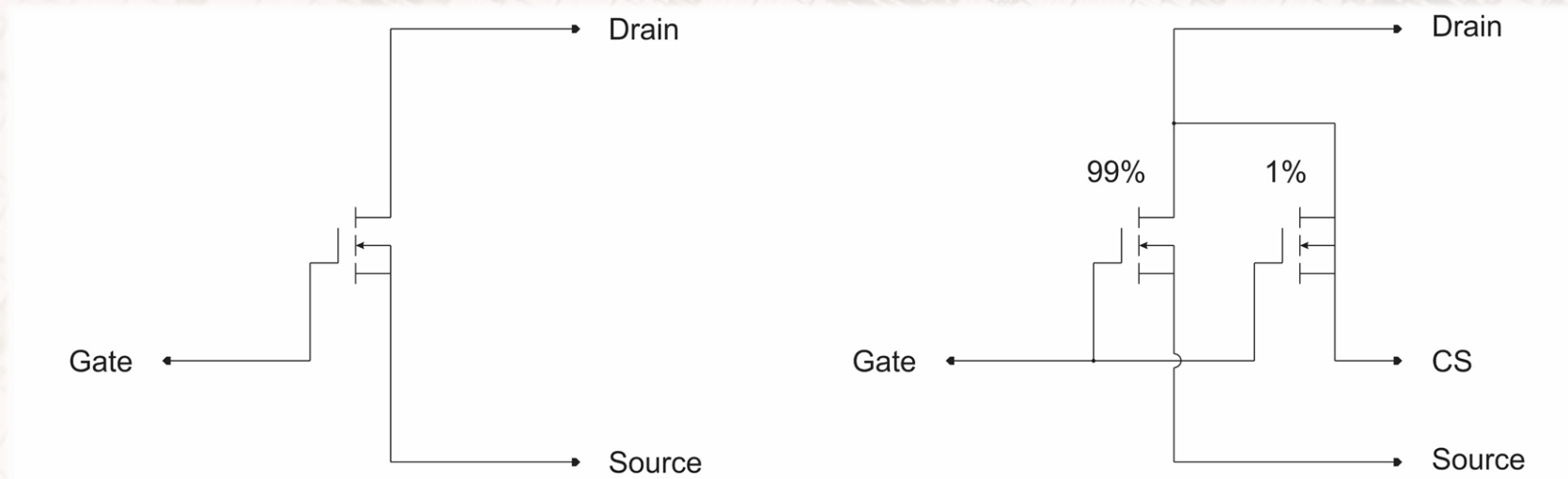
GaN System-on-Chips features

- 4-terminal or 2-terminal temperature sensors



GaN System-on-Chips features

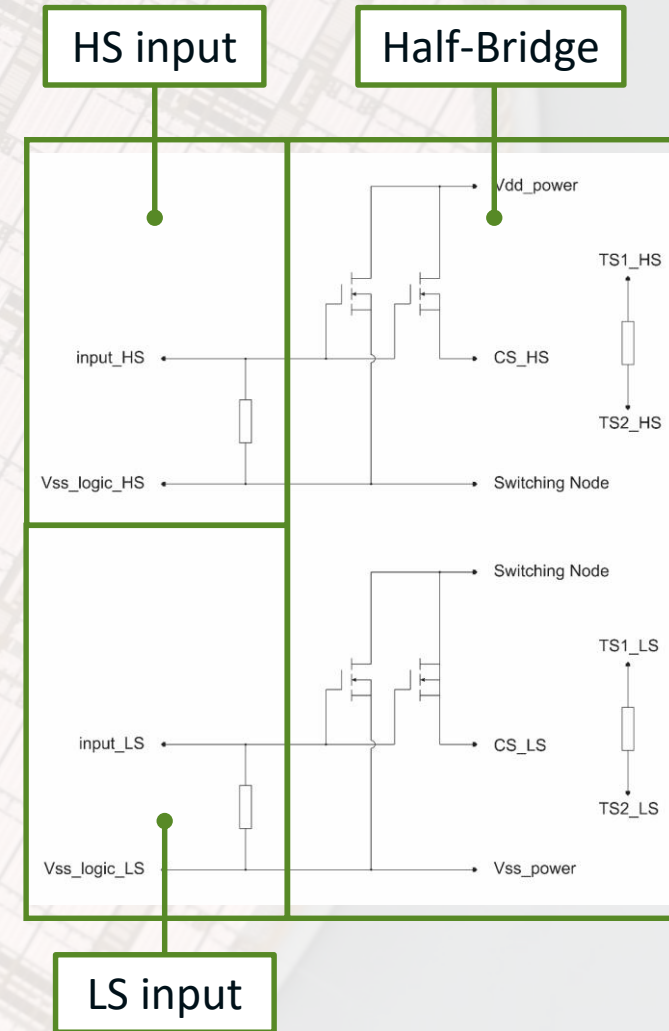
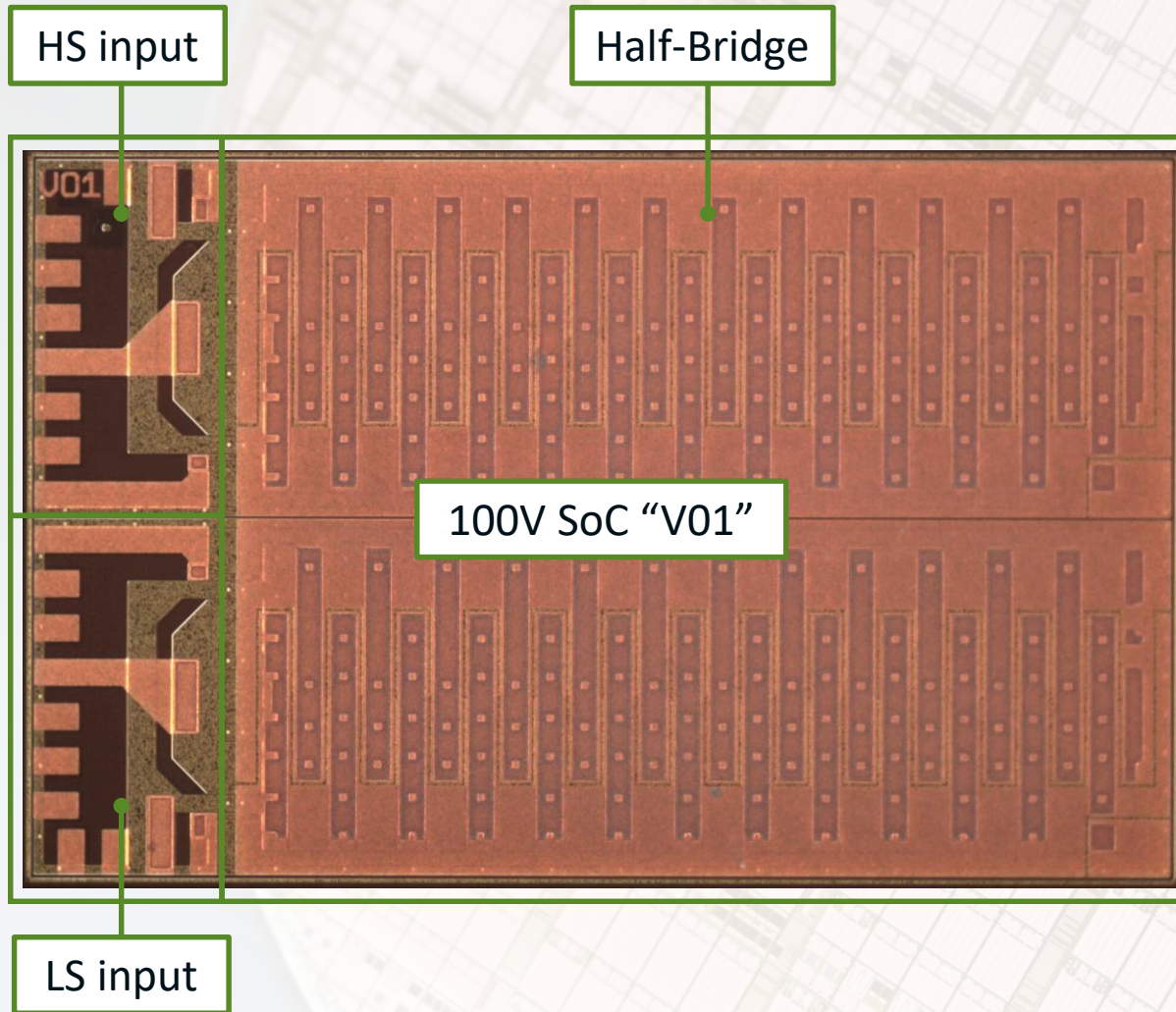
- 1% current-sense terminals



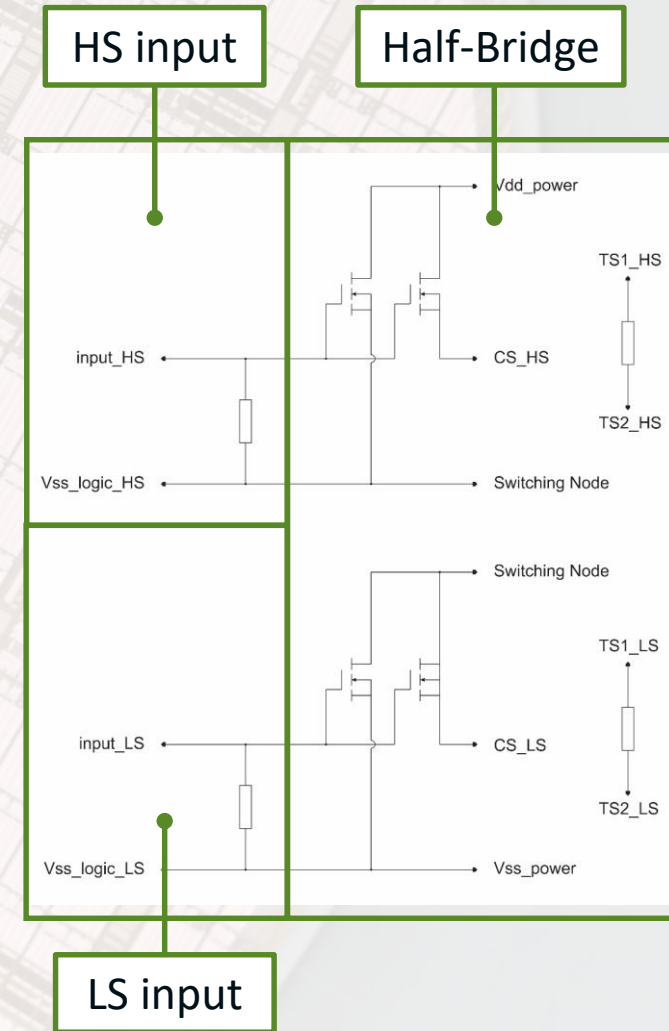
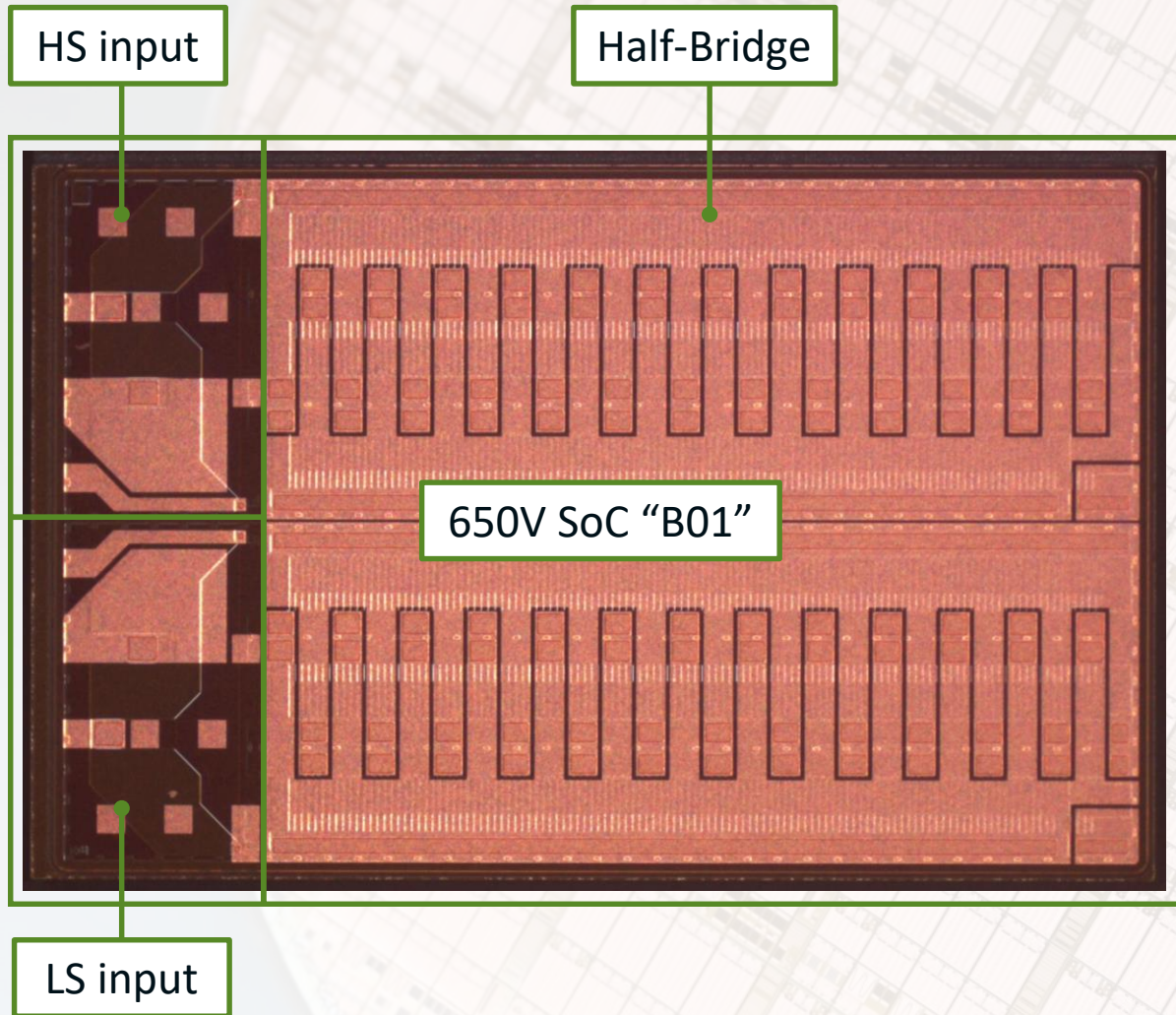
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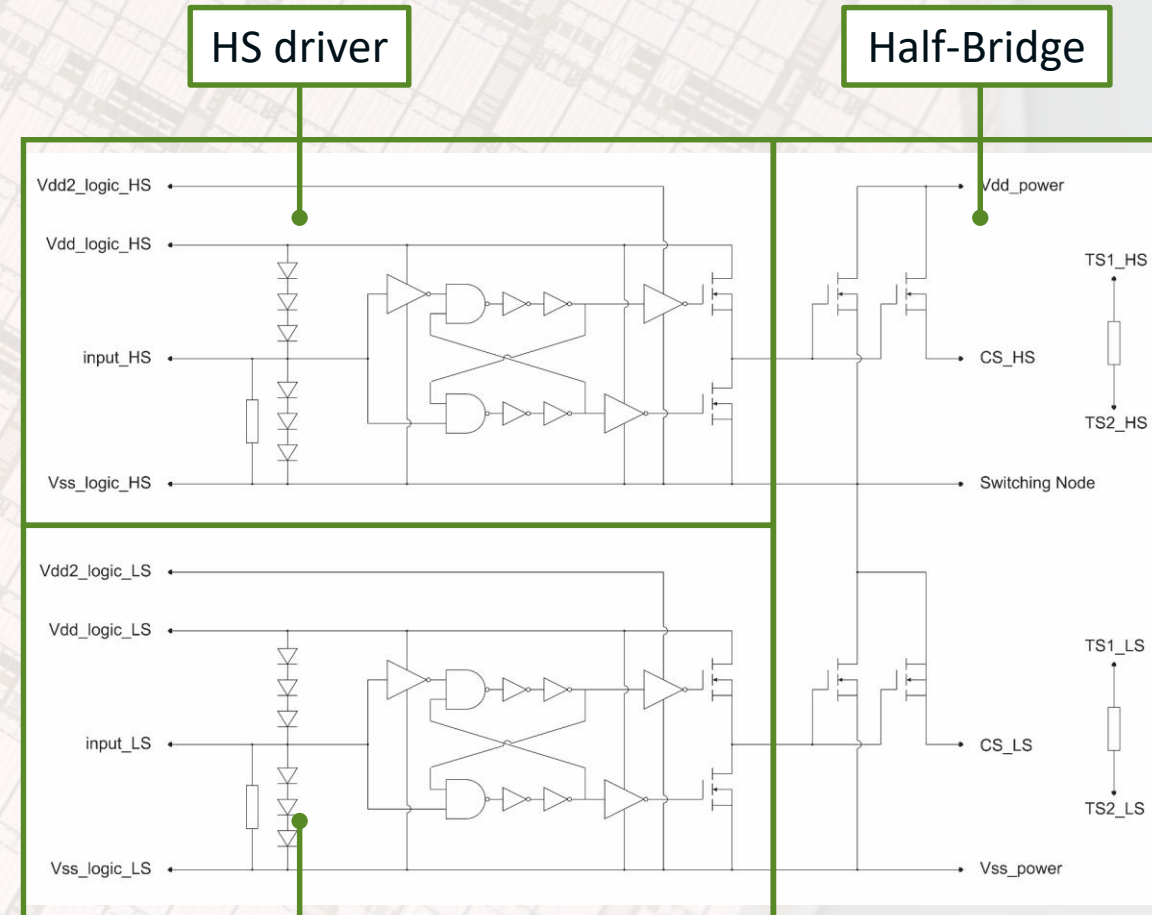
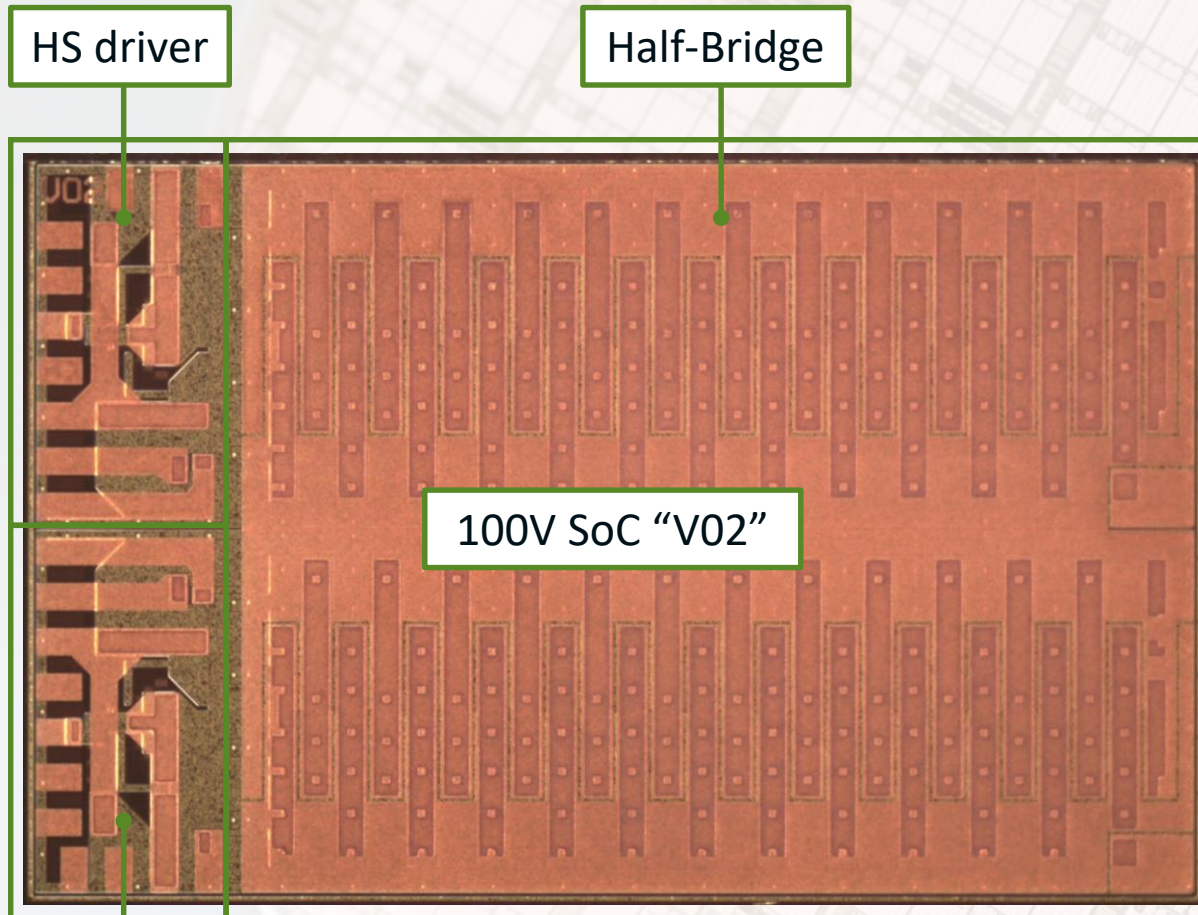
GaN System-on-Chips realisations



GaN System-on-Chips realisations



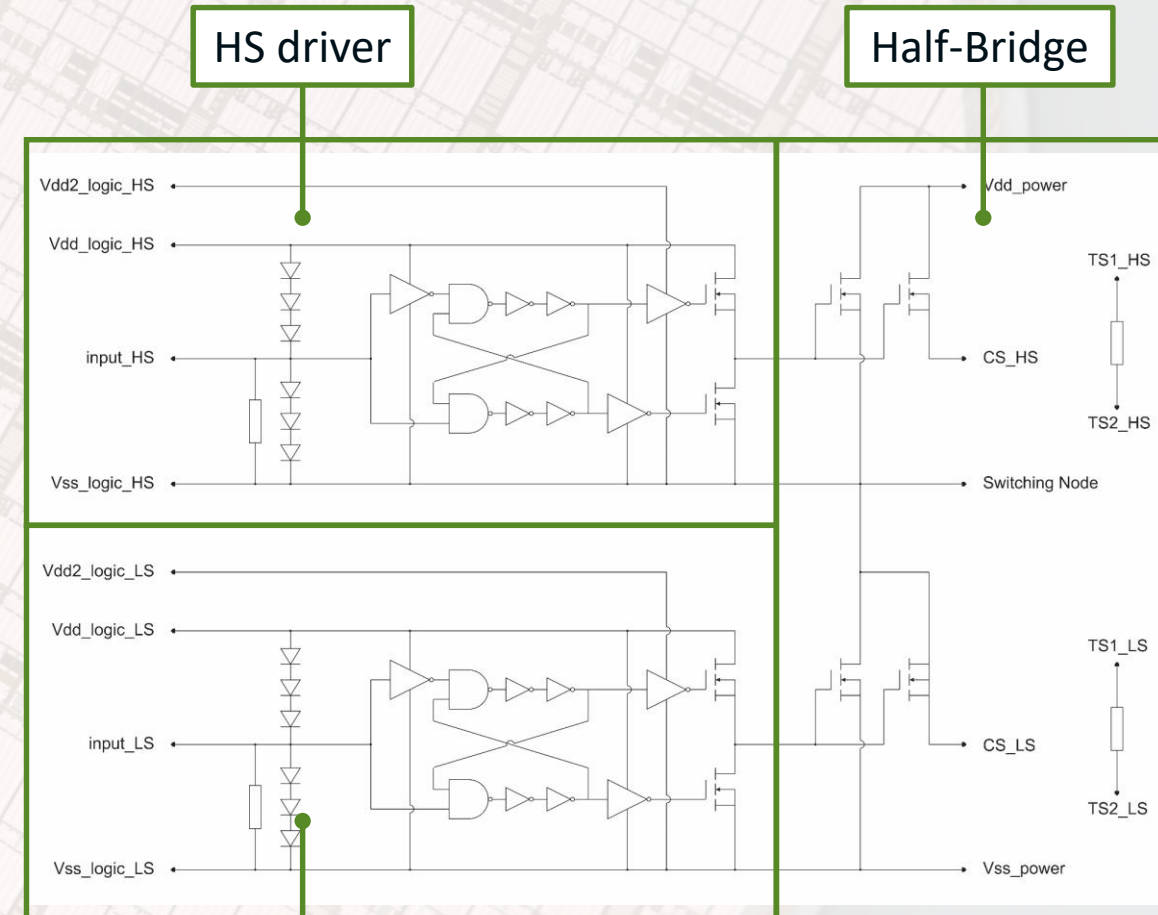
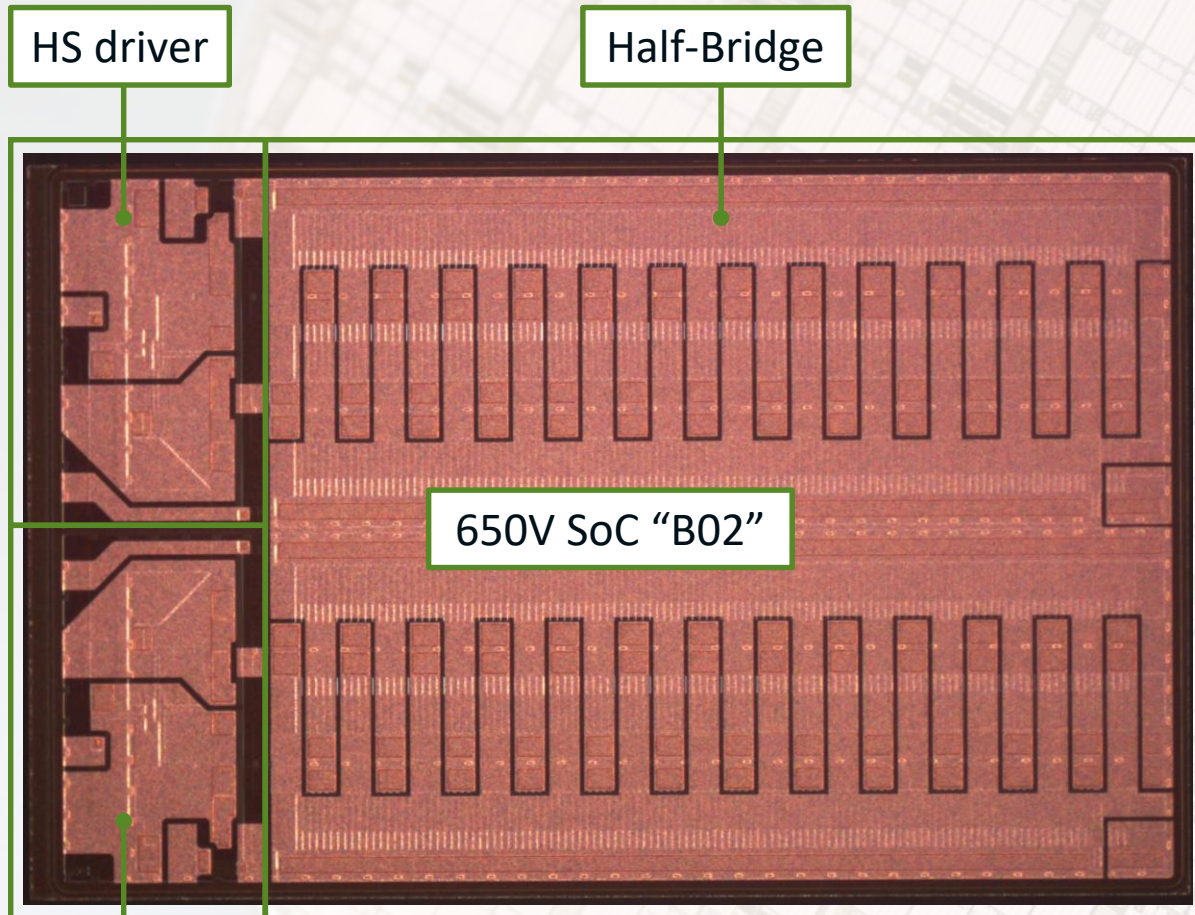
GaN System-on-Chips realisations



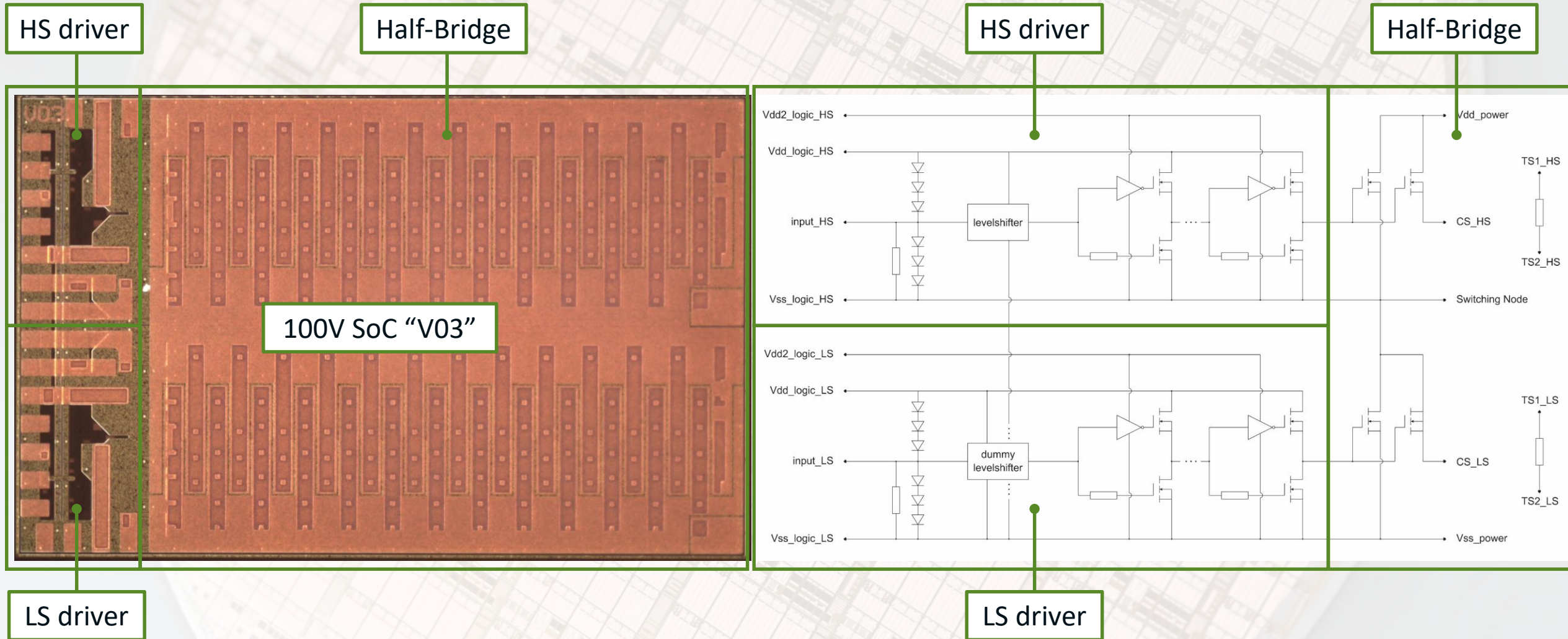
LS driver

LS driver

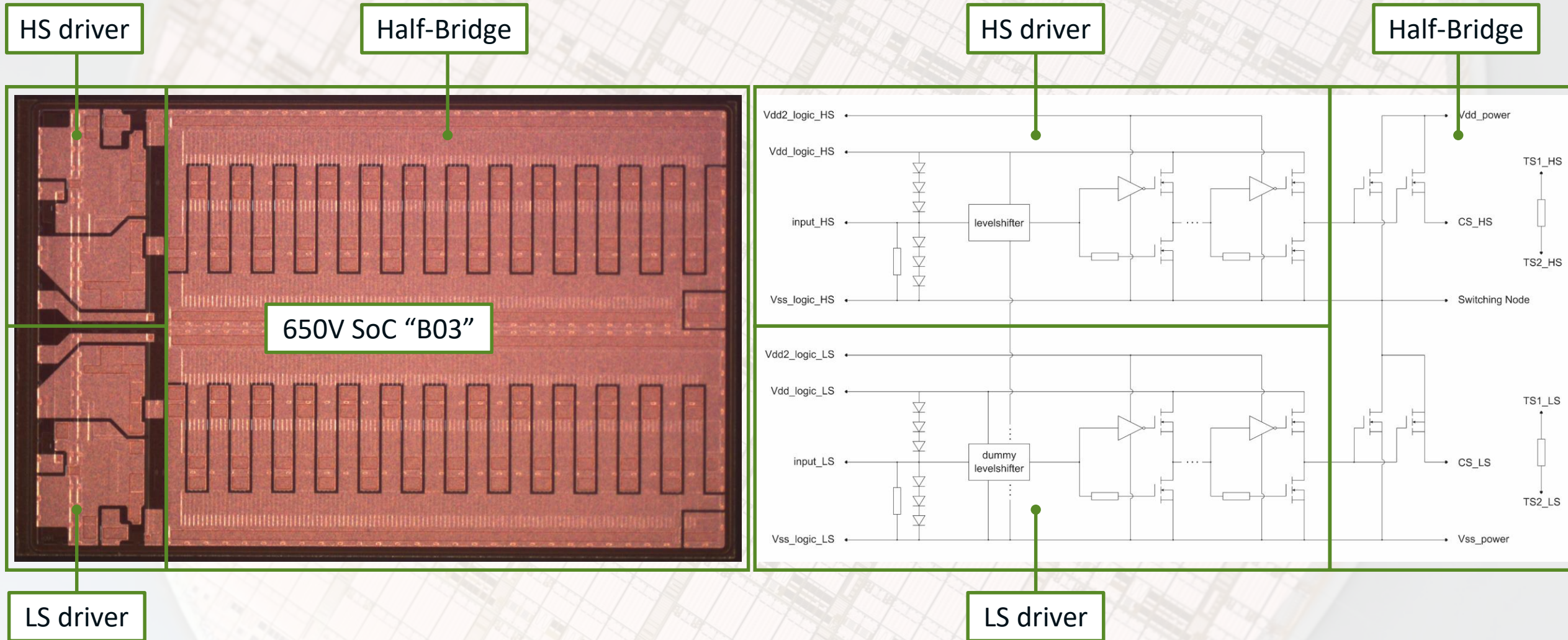
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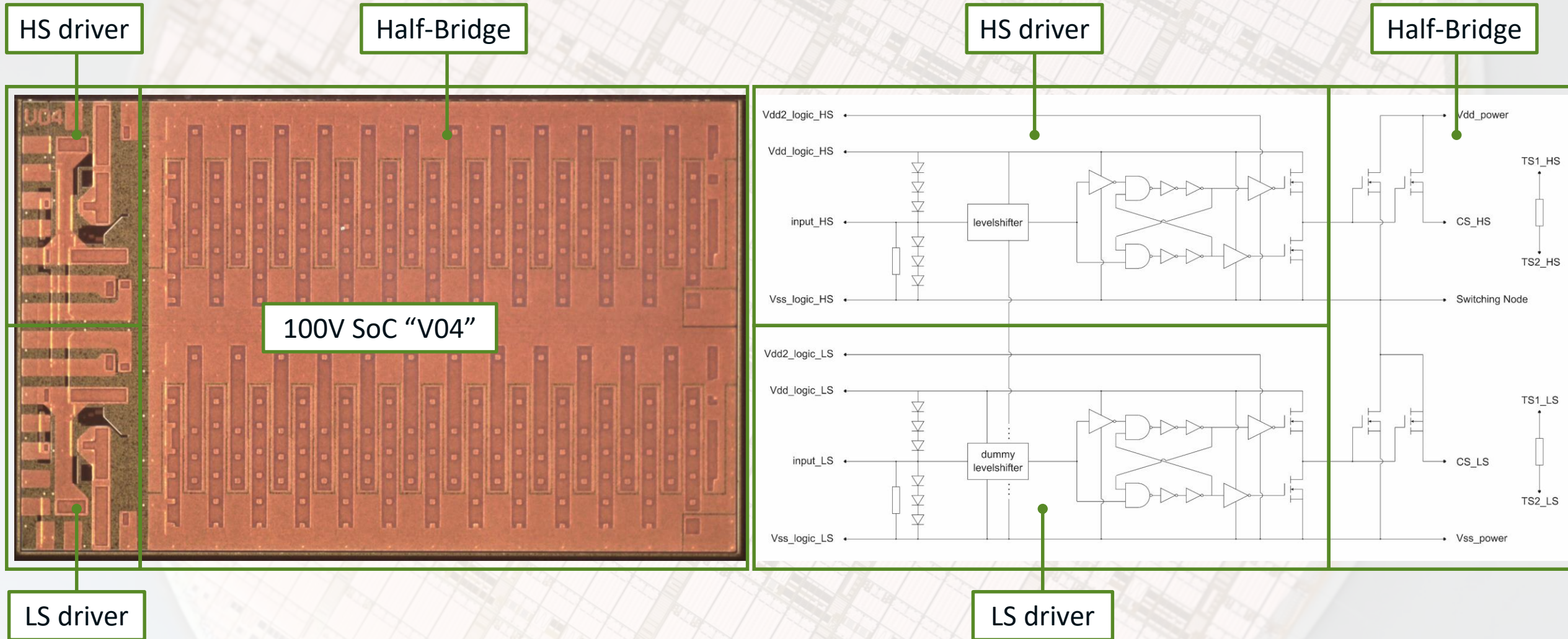
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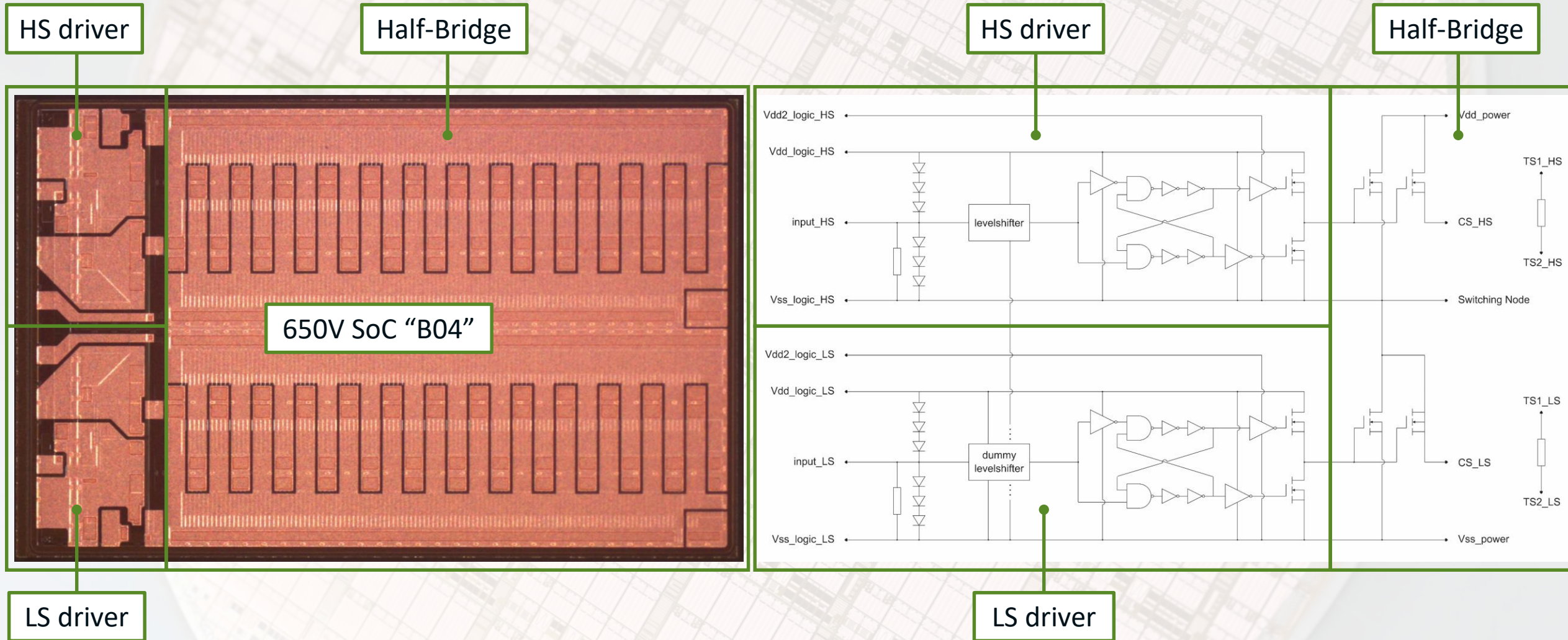
GaN System-on-Chips realisations



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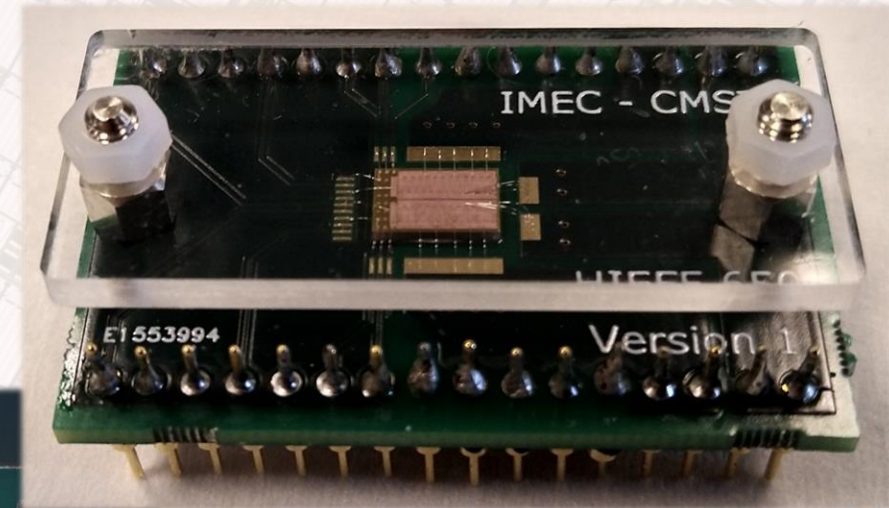
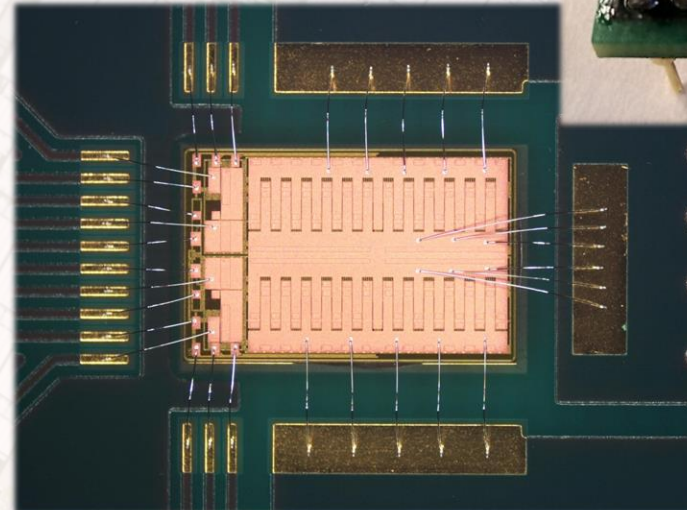


GaN System-on-Chips realisations



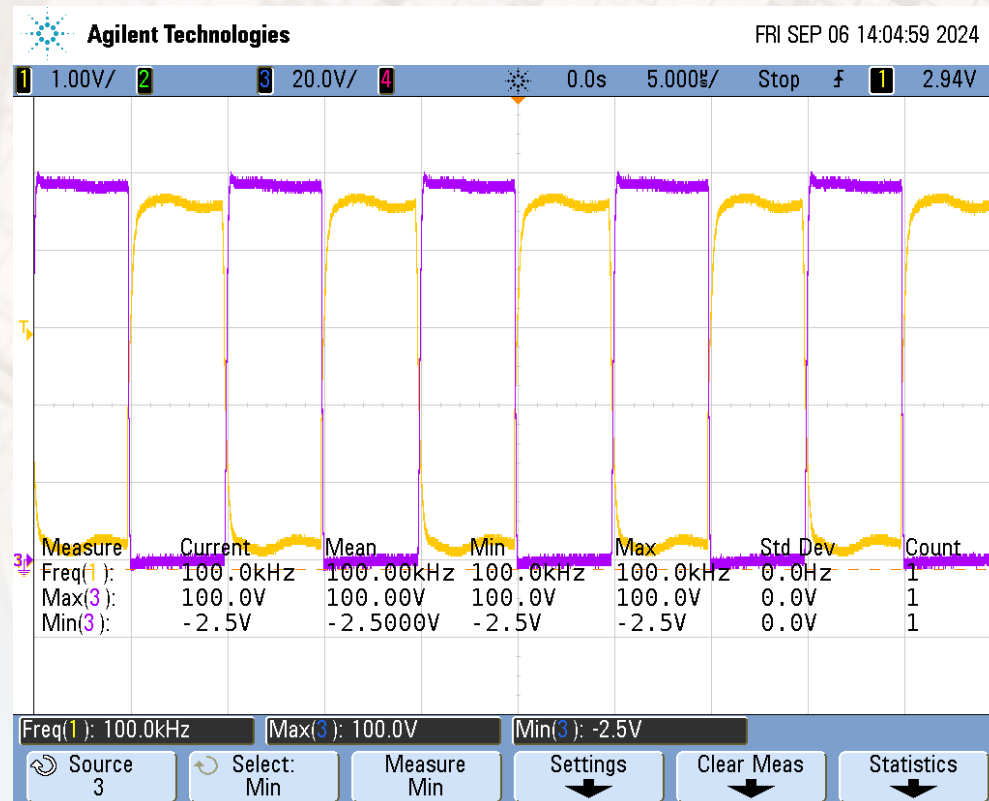
GaN System-on-Chips measurements

- functional measurements
- SoCs wirebonded onto interposer PCB
- current-limiting resistor

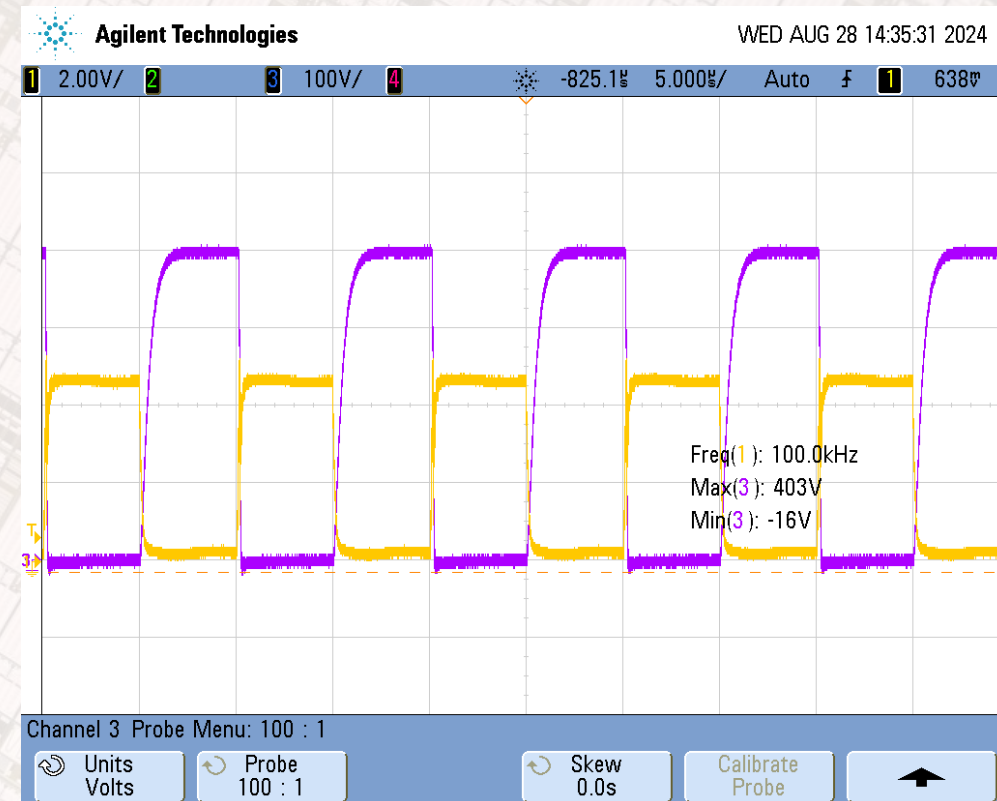


GaN System-on-Chips measurements

- 100V SoC “V01”

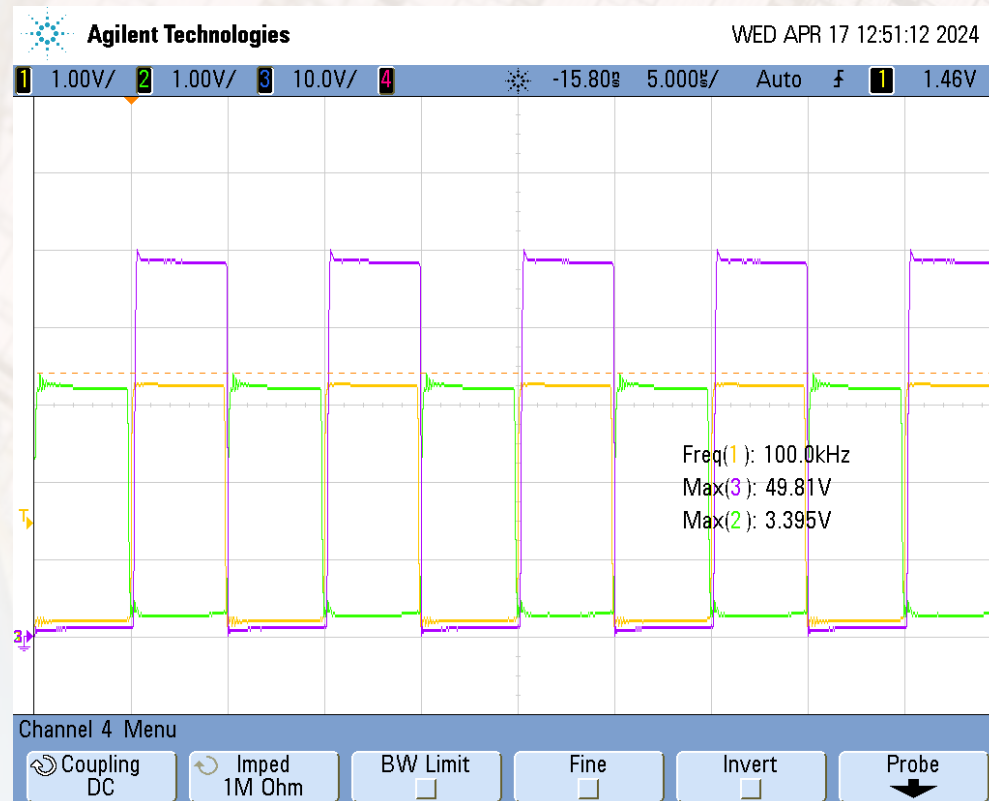


- 650V SoC “V1”



GaN System-on-Chips measurements

- 100V SoC “S8”



- 650V SoC “V3”



End of Presentation – www.HiEFFICIENT.eu