WIDE-BANDGAP TECHNOLOGIES FOR TOMORROW‘S HIGHLY EFFICIENT AND RELIABLE AUTOMOTIVE MOBILITY SOLUTIONS

“Advances in chip embedding and its usage in a 48V inverter application”

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Facts and Figures

2008

Founded

950

Employees

10%

Of turnover invested in inhouse R&D

100%

Integrated into the worldwide AVL network

ONE

Partner as a subsidiary to AVL List GmbH

> 30 M

Vehicles with AVL technology on the road

Global Footprint

7 engineering locations

Global customer support network

6 partner locations inside AVL

As a software and hardware developer we are leading innovation.

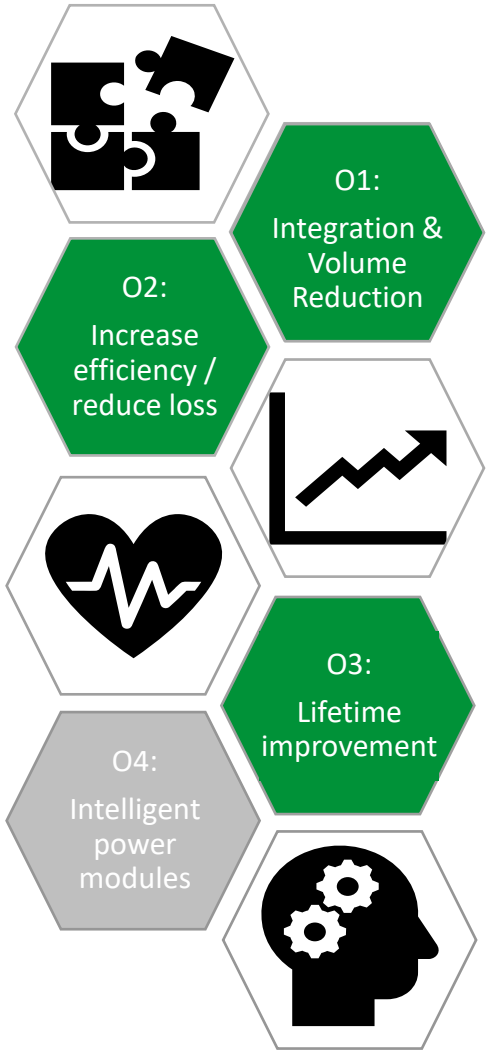
Company Introduction

- AT&S - World Leading High-Tech PCB & IC Substrates Company
  - Founded in 1987
  - Headquarter located in Leoben, Austria
  - ~ 13,500 employees, 7 Locations, 12 plants
  - Among the top ten PCB and IC substrates manufacturers worldwide
  - Focused on Classic PCB, High-end PCB, IC substrates and Advanced Packaging

- Website: www.ats.net

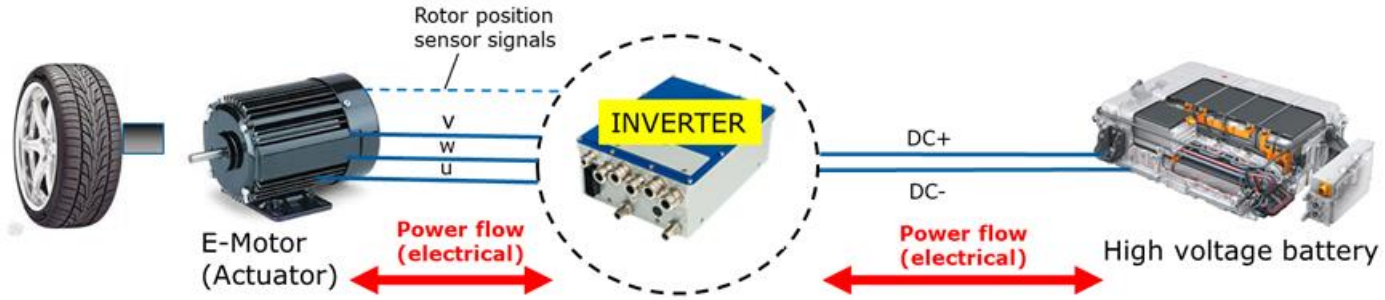
UC3 – 48V High Power GaN Inverter

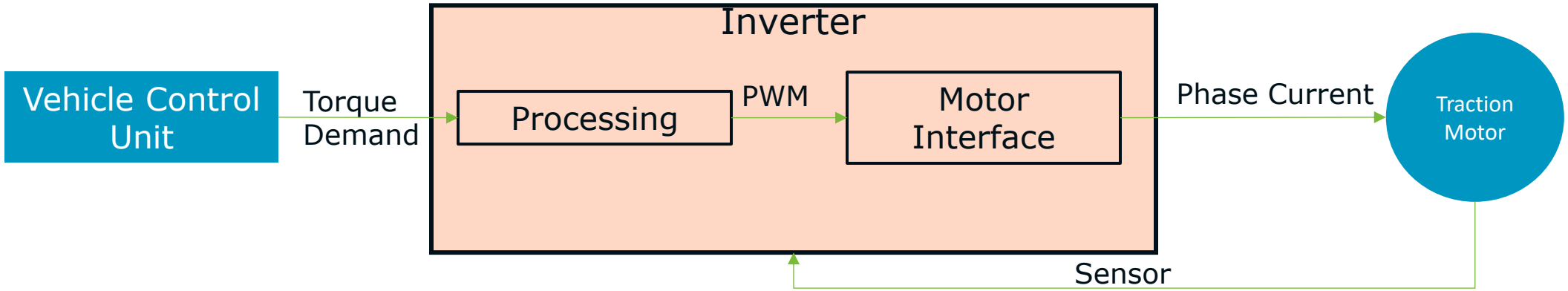
- The objectives of this use case are
  - **Reducing weight and volume** of automotive applications by reducing the converter designs by a factor of 10% and additionally enabling **unshielded cables**
  - **Improve efficiency** to achieve a target of 98%
  - **Improve lifetime and reliability** of the power stage and the mechanical design



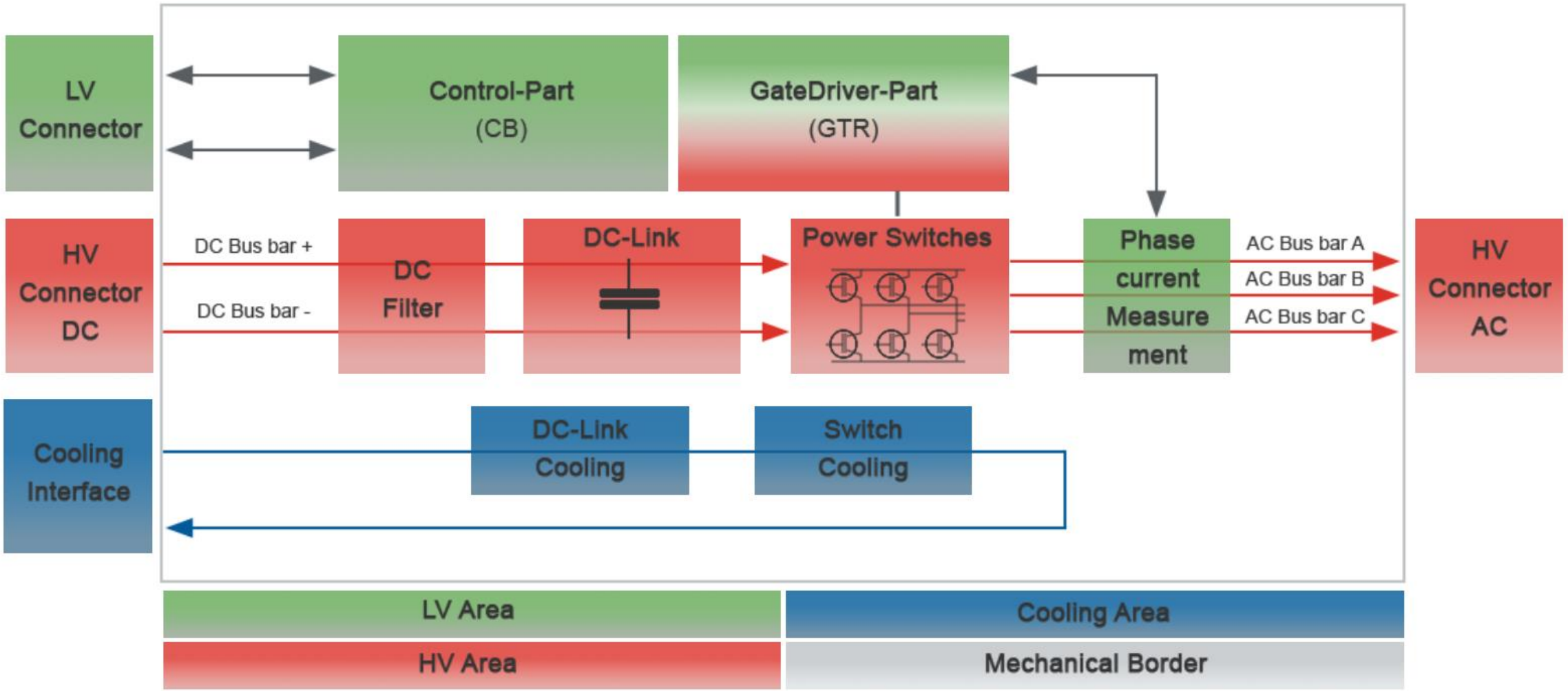
Traction Inverter

Electrical Drivetrain



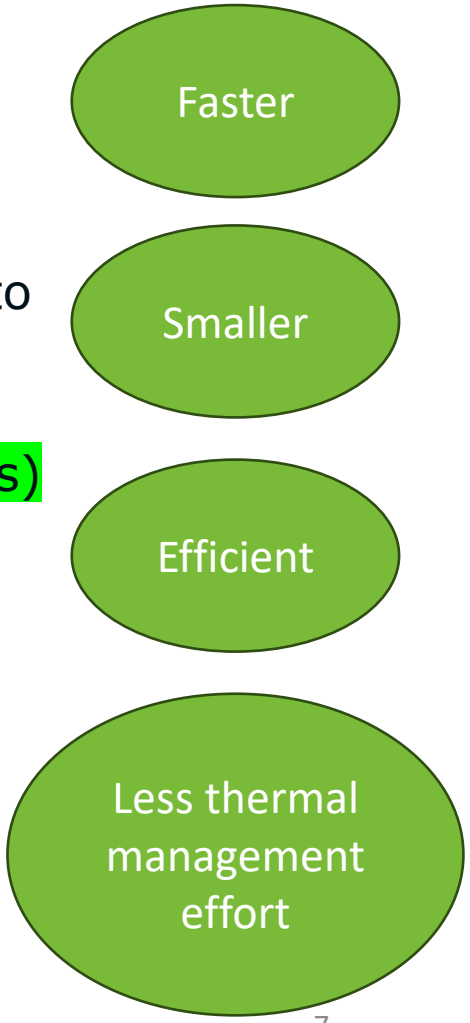


Inverter Architecture



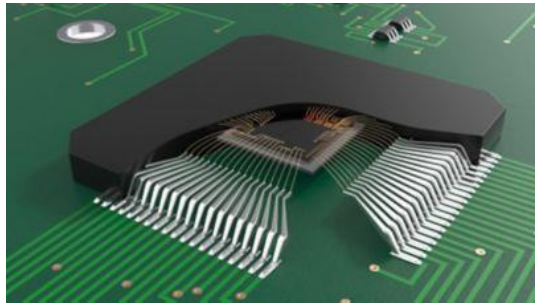
Advantages of GaN

- Gallium nitride can conduct electrons more efficiently
  - → 10 times shorter switching time than Si MOSFETs
- Lower on-resistance per unit area for the same voltage rating compared to both SiC and Si
  - → Lower switching loss and less EMI noise
  - → Reduced size (5 to 10 times smaller than Si MOSFETs and IGBTs)
- The thermal resistance is lower than Si devices
  - → Better thermal performance



Advantages of Embedded Die Packaging

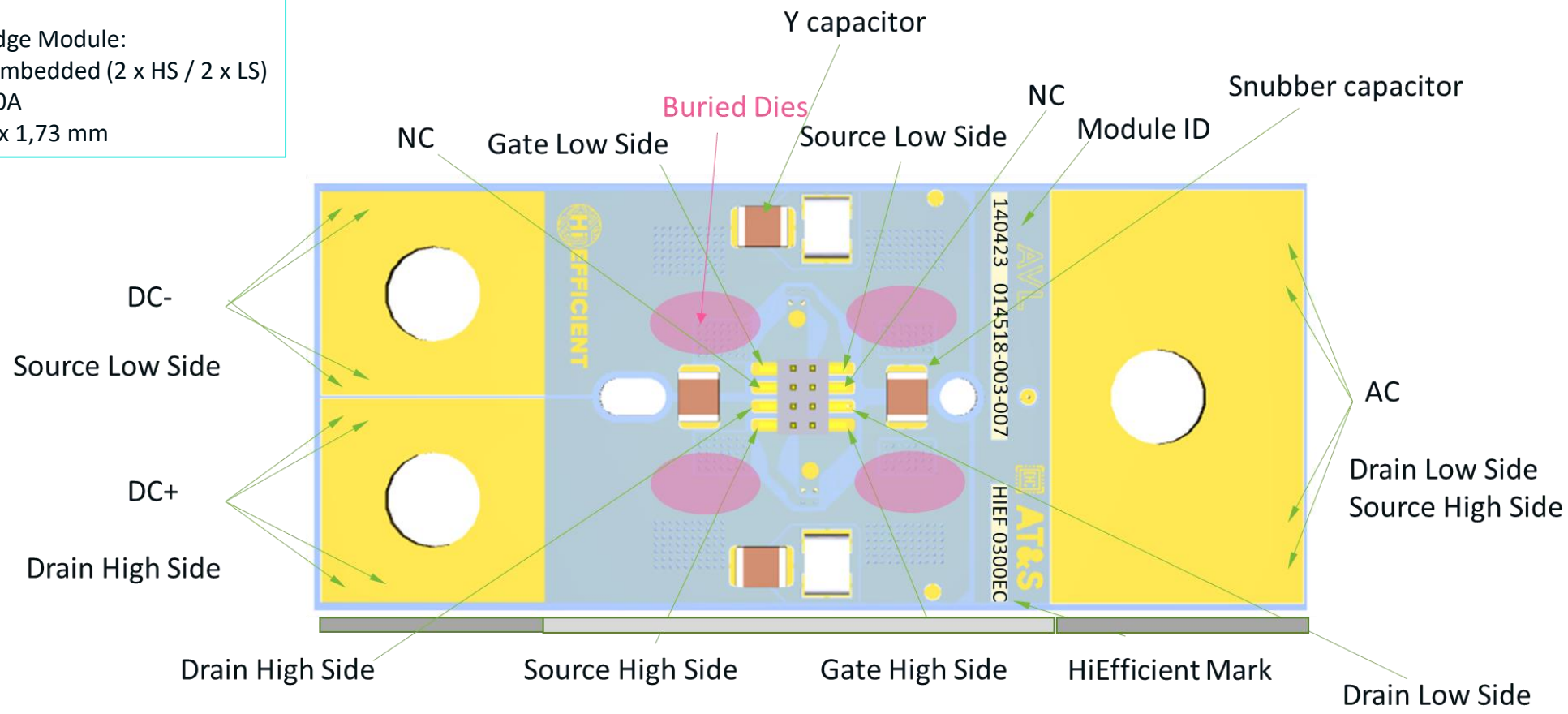
- Shorter interconnections
  → Minimizes distortion and power loss
- Stable Cu interconnections
  → High mechanical stability
- Lower thermal resistivity
  → Better thermal performance
- Design flexibility



*https://www.microsemi.com/company/technology/embedded-die-technology

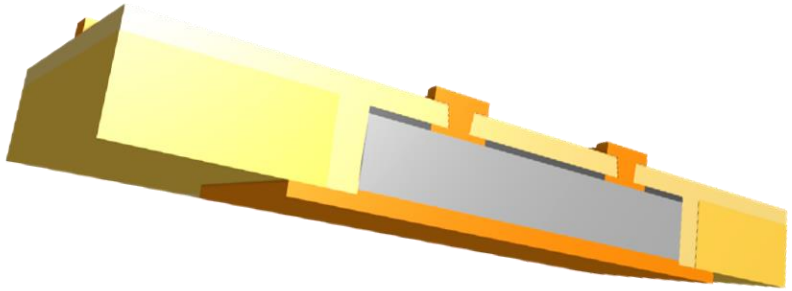
GaN Power Module Description

Half Bridge Module:
4 GaN embedded (2 x HS / 2 x LS)
80V, 180A
67 x 29 x 1,73 mm



AT&S ECP® Technology

PARSEC
The preferred packaging technology for high – voltage applications with double-sided component connection and optimized thermal performance



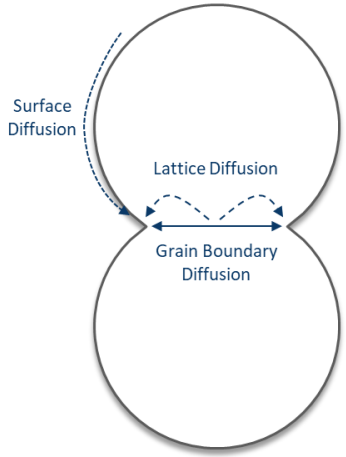
Component Type	Actives – RDL mandatory
Min. / Max. Component Size	1x1mm² – 8x8mm²
Min./Max. Component Thickness	150µm – 300µm
Min. Component Pad Size /Min. Connection Diameter	Standard: 300µm / Ø150µm \\ Advanced: 270µm / Ø120µm
Min. Component Pad Pitch	Actual pad size + 100µm (sub)
Component Pad Metallization	Copper only
Component Connection	Double-sided
Component Fan-out Concept	Laser, Galvanic, Lithographic
Max. Die to Package Ratio	30%

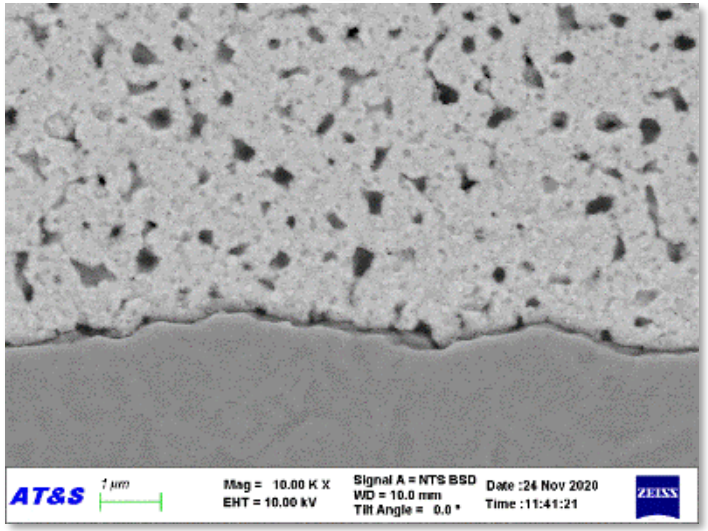
RDL … Redistribution Layer

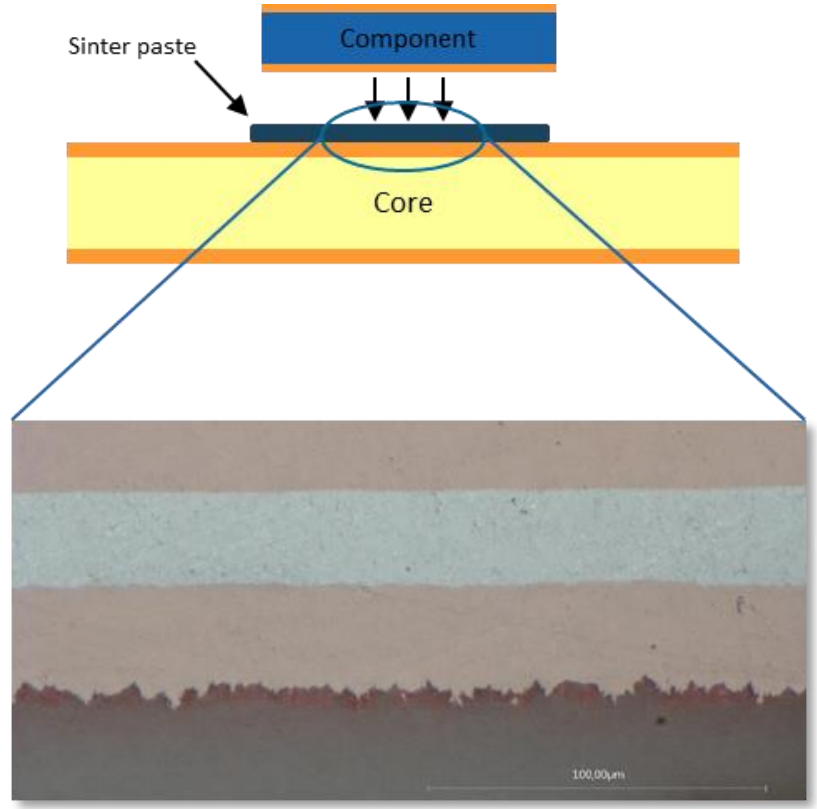
Parsec … Planar Surface Embedding Components

Sinter Lamination Technology

- Evaluation show many Ag sinter paste are compatible with Cu terminated components

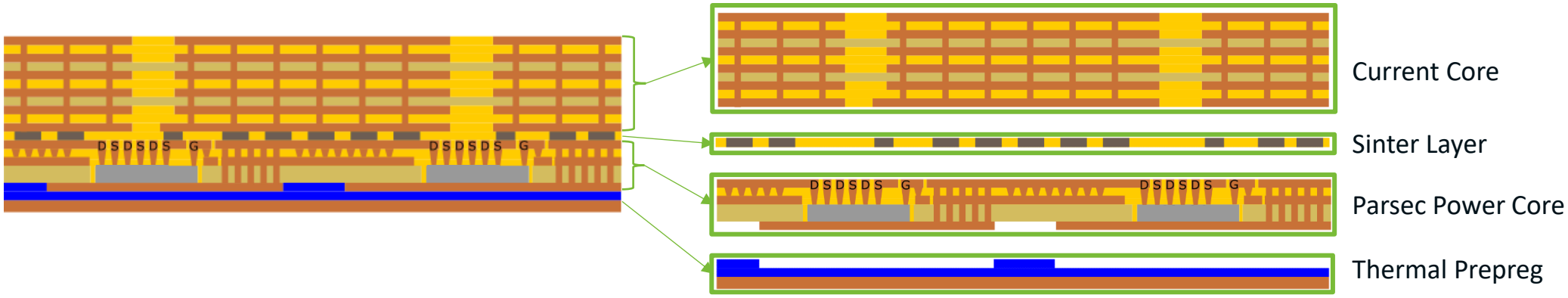






- SEM picture Ag-sintered interfaces Ag – Cu after TCT:
  - Low porosity Ag-layer
  - No voiding in interface
  - No delamination in interface

Construction of the Power Module



Step 1: Parsec Power Core and Current Core are fabricated separately

Step 2: Both Cores are laminated and sintered together

Step 3: Thermal Prepreg is laminated on the bottom side

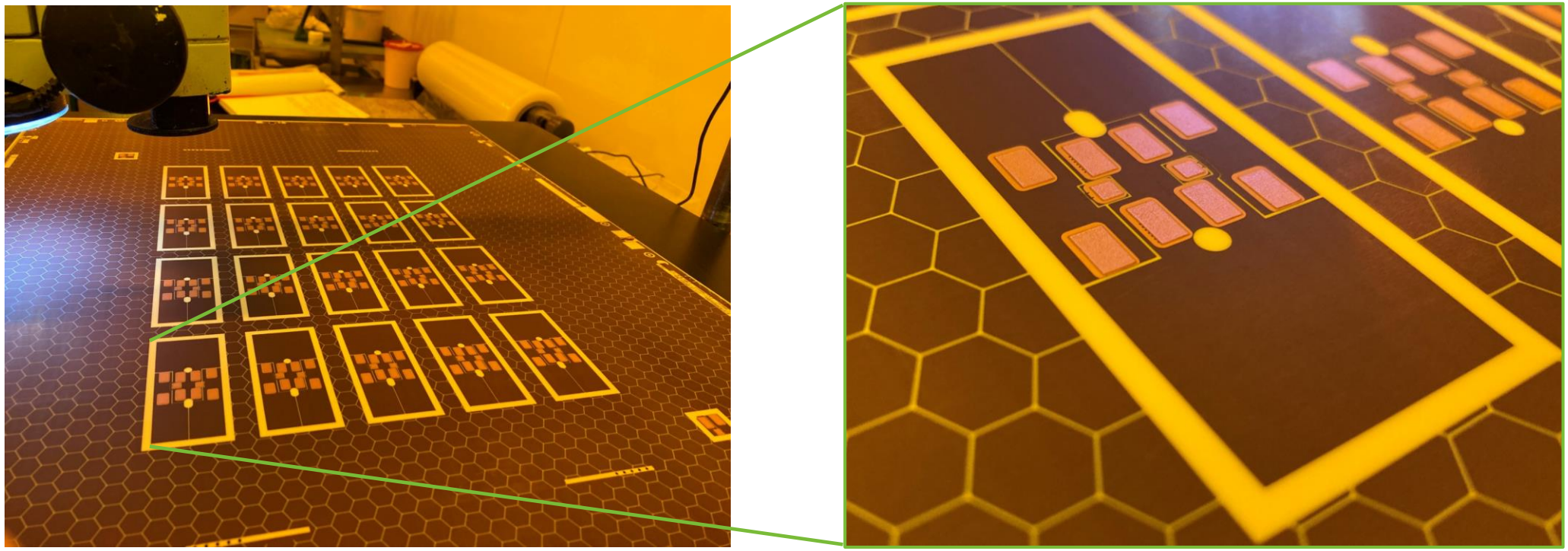
➔ Reduction of parasitic inductances to enable fast switching and **increase efficiency & lifetime**

➔ Improvement of thermal performance and Miniaturization enable higher **power density**

Construction of the Power Module

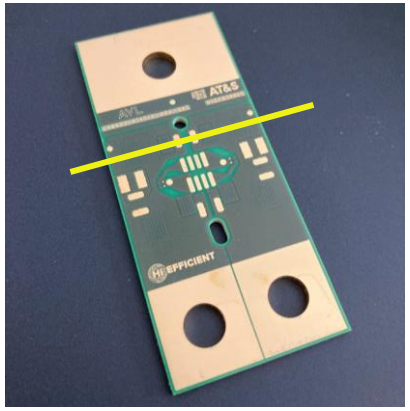
Copper based Sinter depots

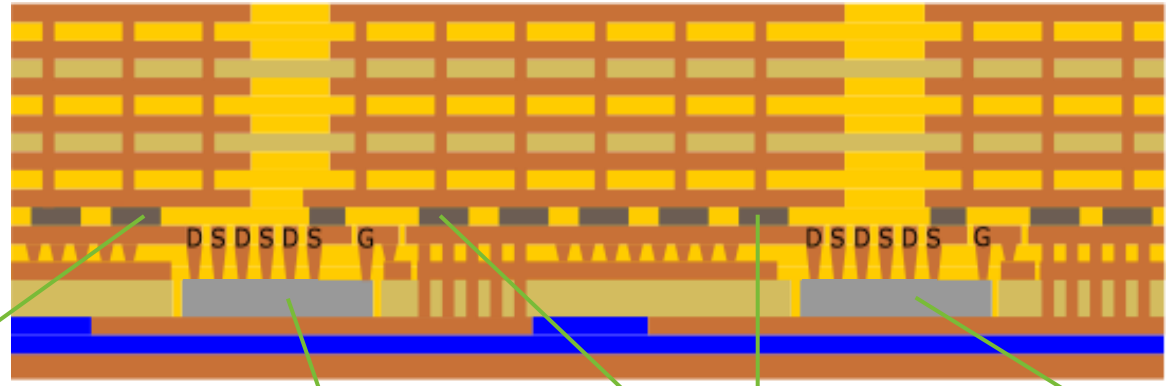
- The copper based sinter lamination is a novel technology developed in HiEFFICIENT project and these half bridge modules provide the first functional demonstrators.

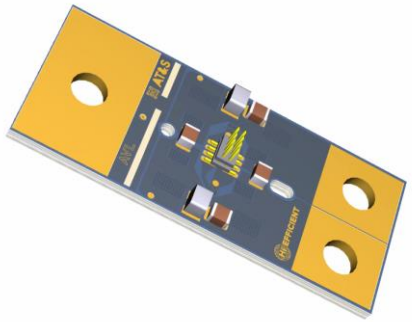


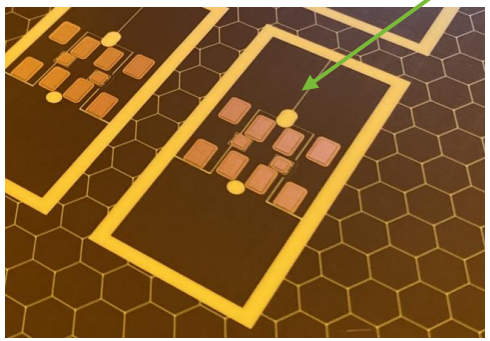
Half Bridge Module

Cross - section





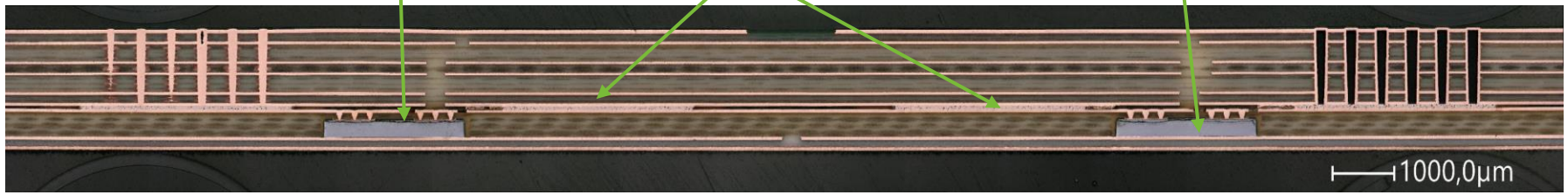




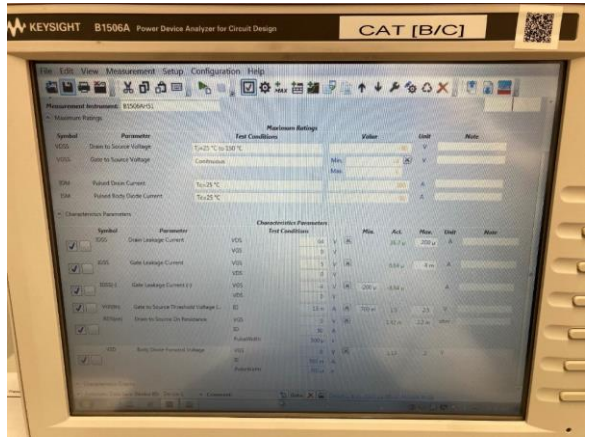
GaN High Side

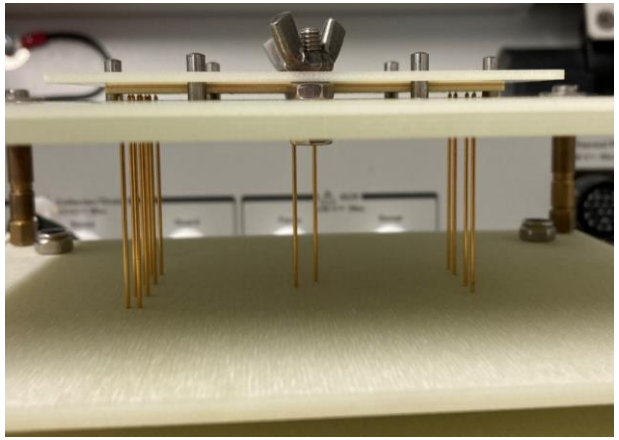
Sinterdepots

GaN Low Side



Static Electrical Characterisation

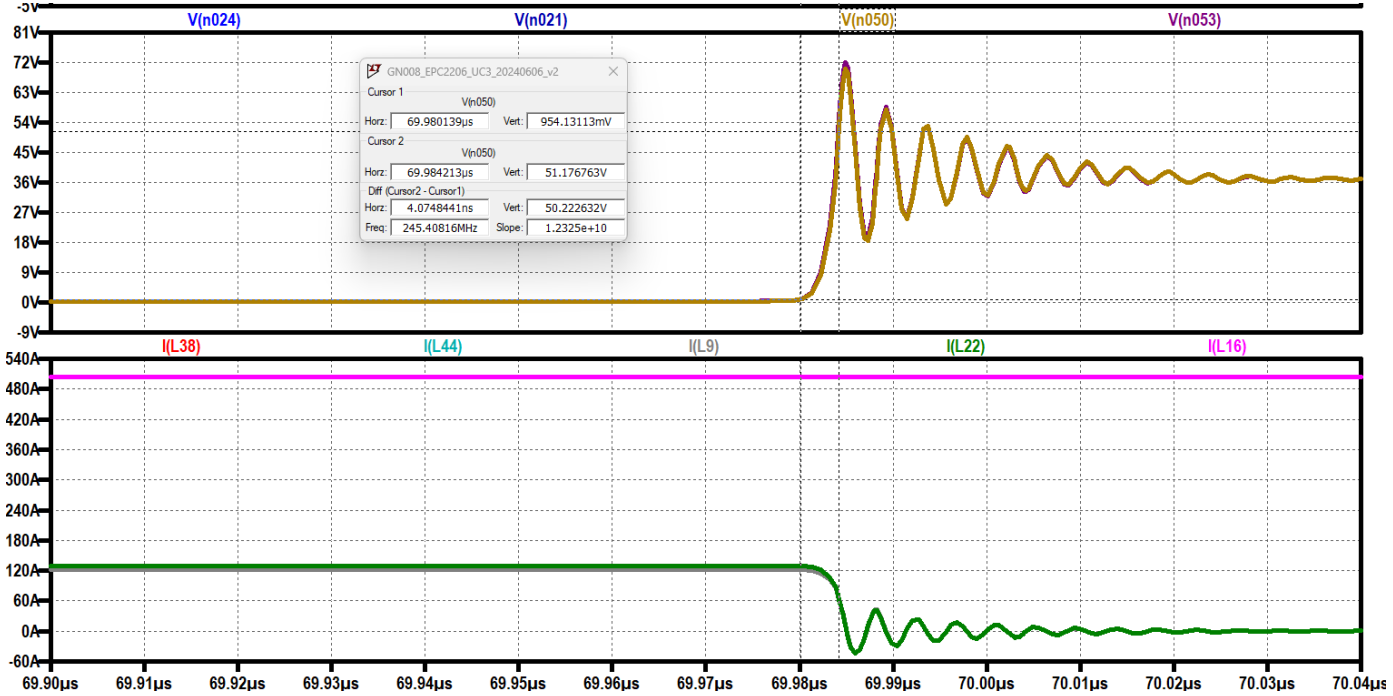


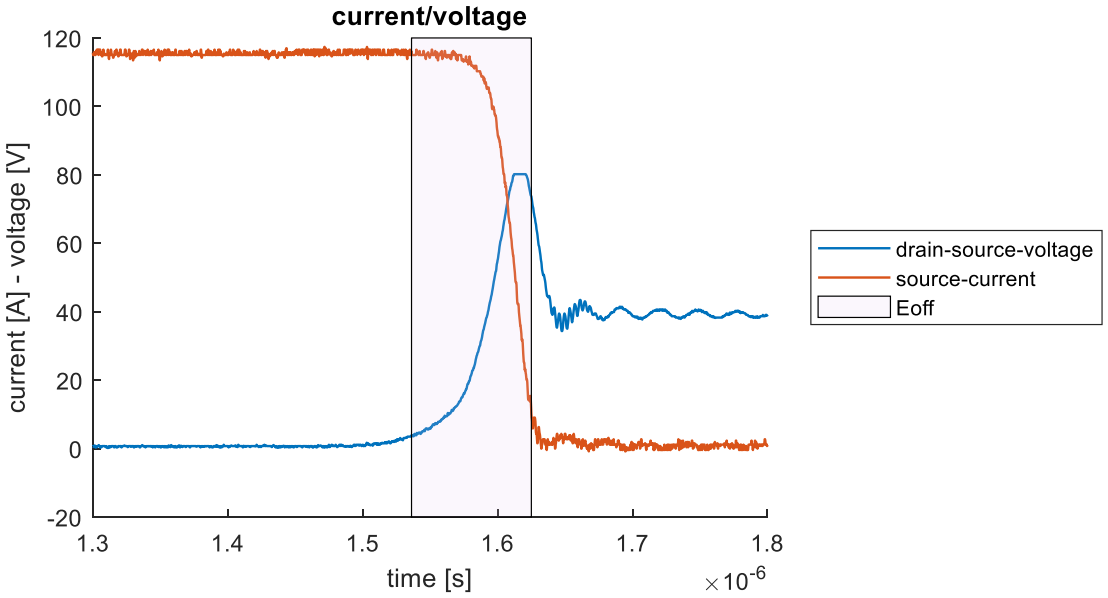


Parameter	Datasheet	Unit	Test Condition	Results (mean of 100 measured modules)
$R_{DS(on)}$	1,1 max. 1,95 max.	mOhm (components) mOhm (+Module +parasitics)	V_{GS}=5V ; I_D=50A PW=500µs	1,44
I_{DSS}	400 max.	µA	V_{DS}=64V ; V_{GS}=0V	31,06
I_{GSS}	400 typ. 8000 max.	µA µA	V_{GS}=5V V_{DS}=0V	4,63
$I_{GSS(-)}$	-40 typ. -400 max.	µA µA	VGS=-4V ;V_{DS}=0V	-5,51
$V_{GS(th)}$	1,2 typ. 2,5 max.	V	V_{DS}=V_{GS} ; I_D=13mA	1,39
V_{SD}	1,5 typ.	V	V_{GS}=0V ; I_F=0,50A ; PW=500µs	1,13

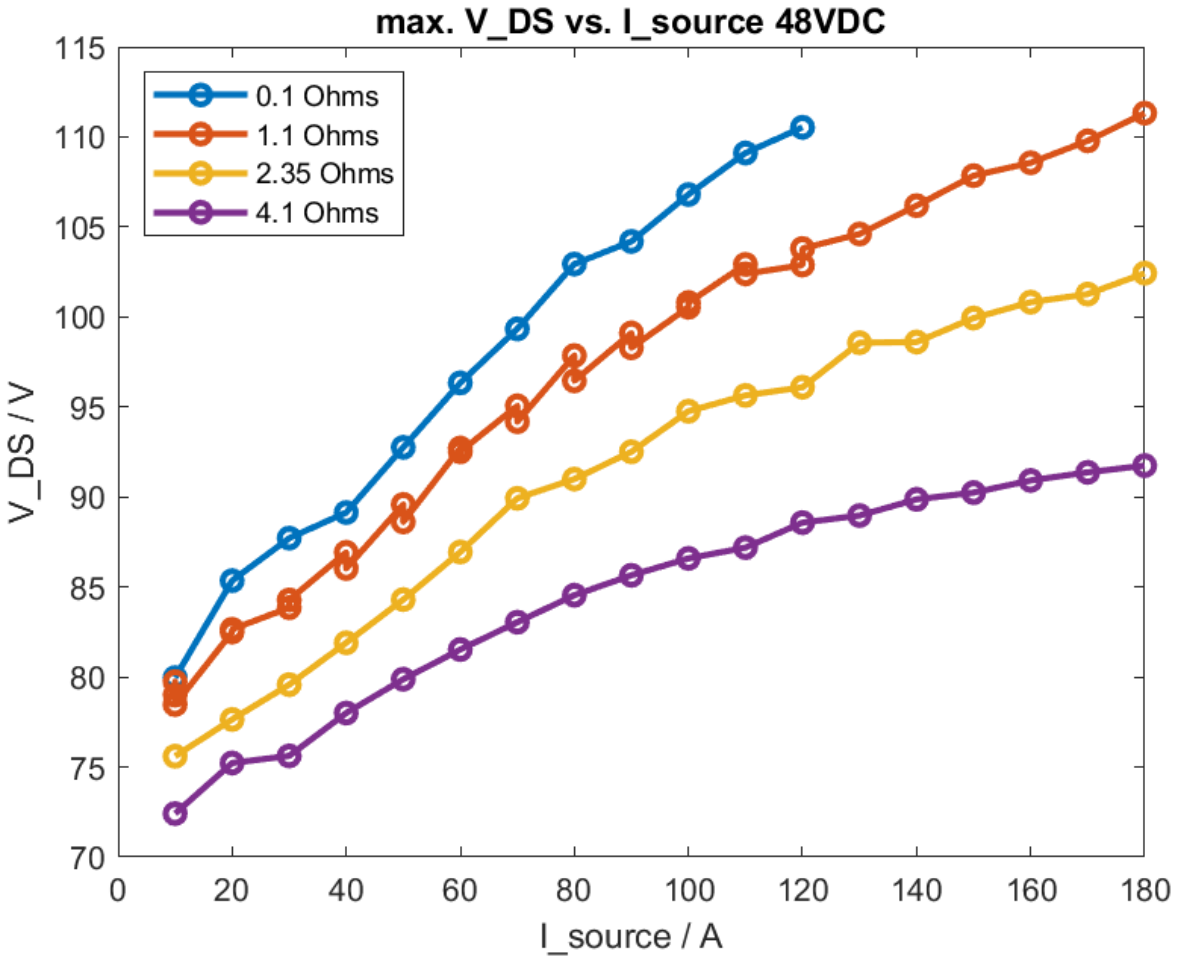
UC 3 – DPT Simulation vs. Measurement

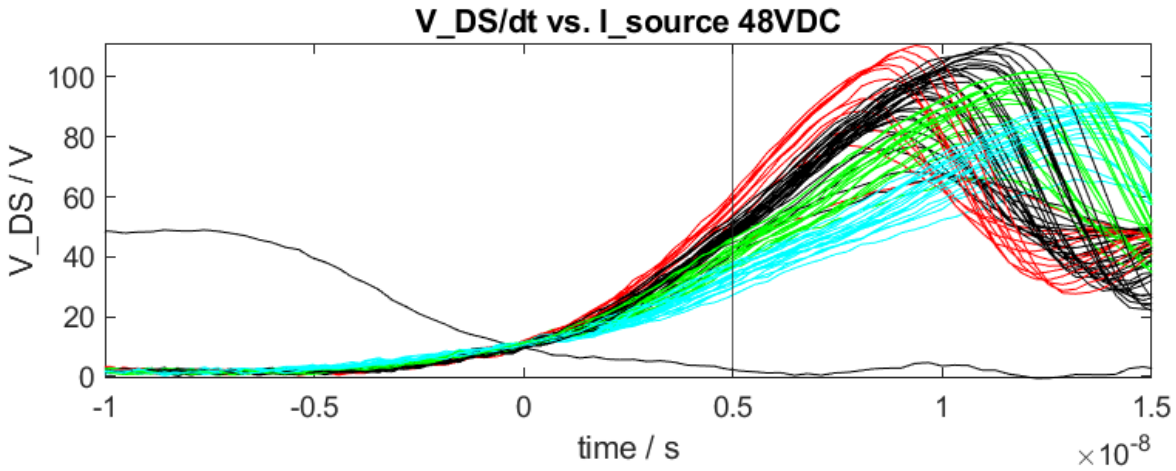
Turn-off transient





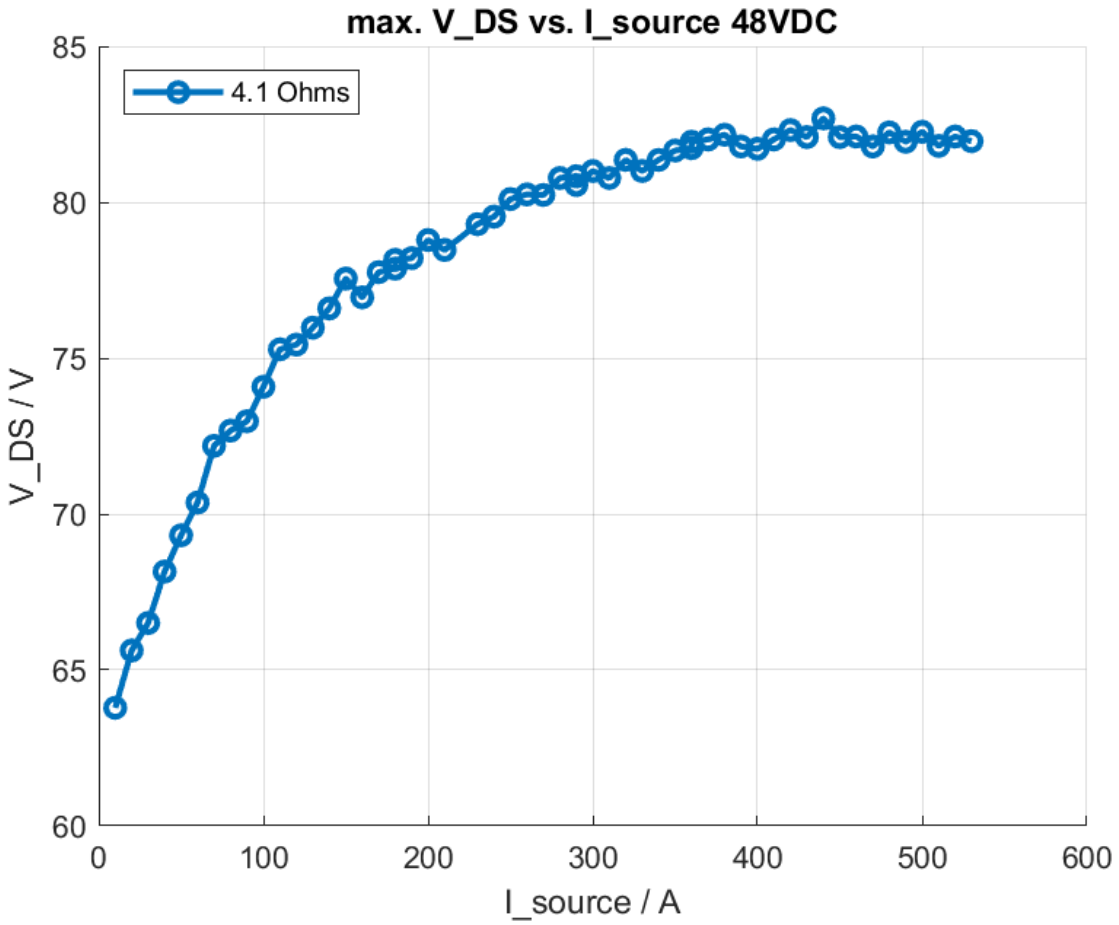
Double Pulse Test Results/Single Module

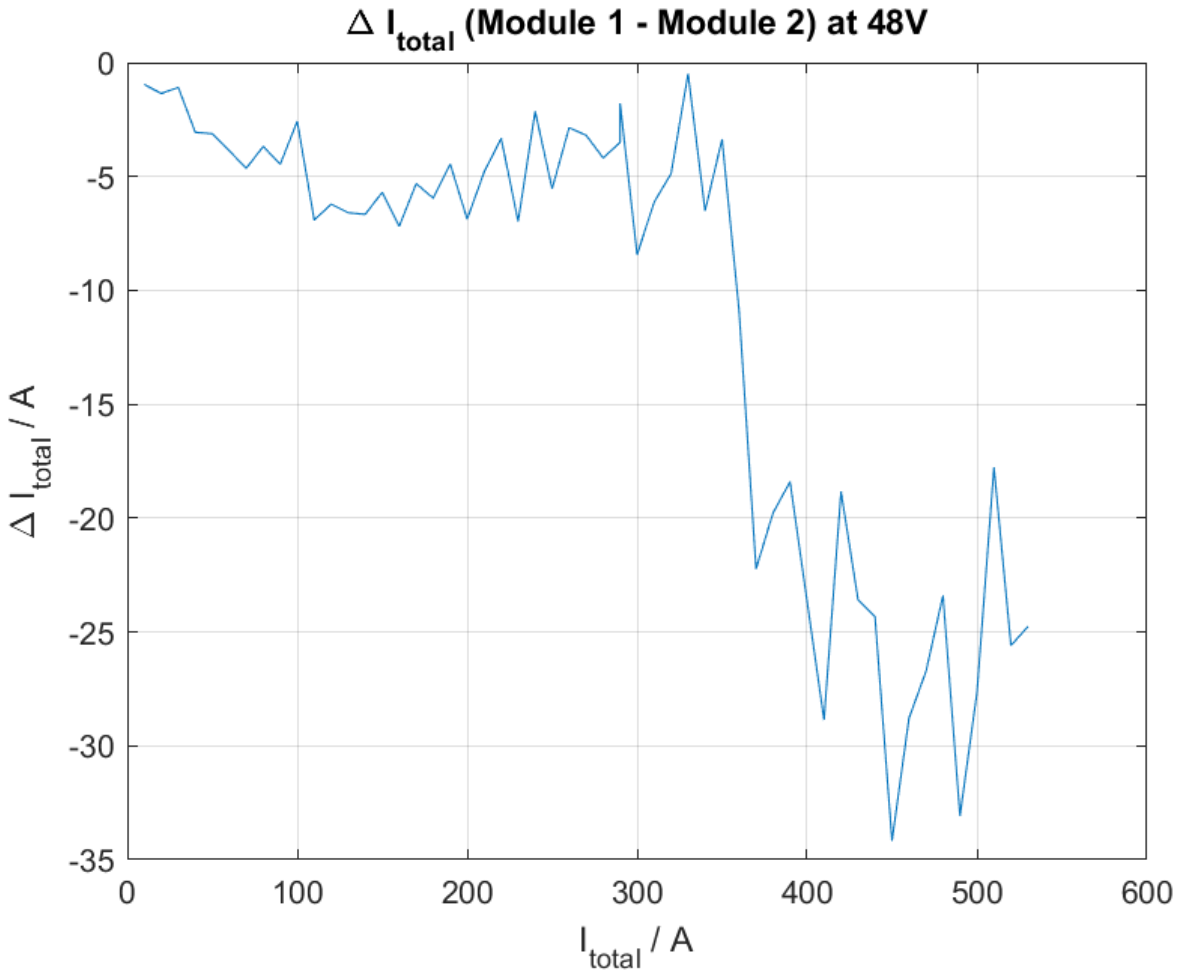




Rgoff	Max. dV/dt
• 0.1 Ohms (red)	13.28 V/ns
• 1.1 Ohms (black)	10.83 V/ns
• 2.35 Ohms (green)	9.08 V/ns
• 4.1 Ohms (cyan)	7.45 V/ns

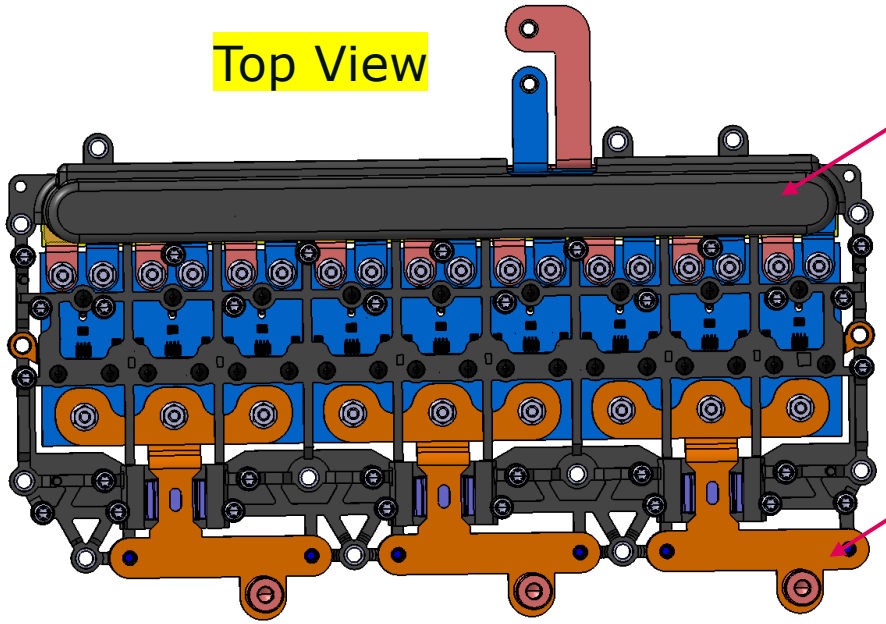
Double Pulse Test Results/ Two Modules





Power Module Assembly

Top View



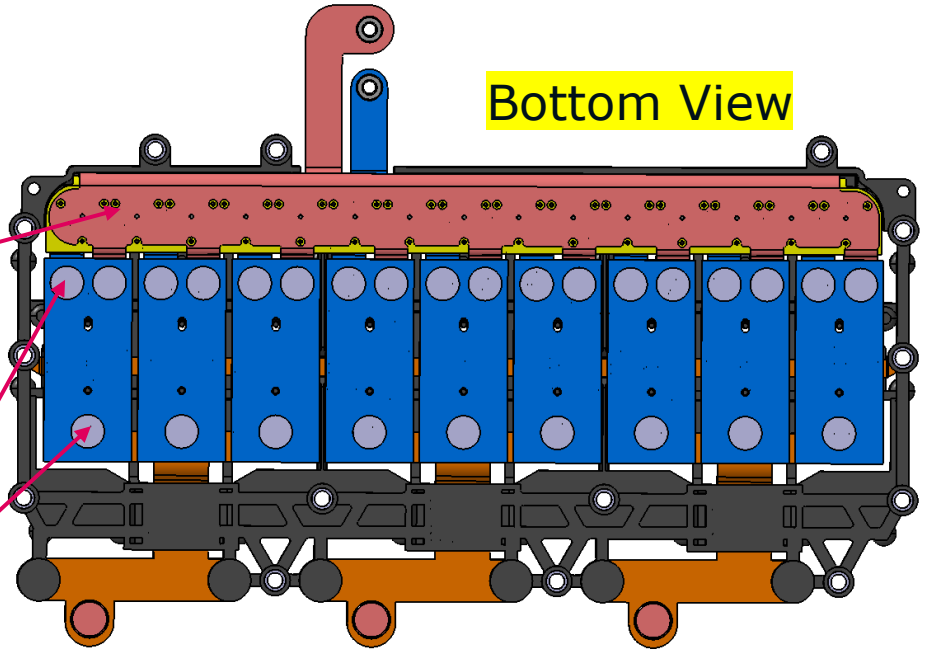
Power Module Carrier

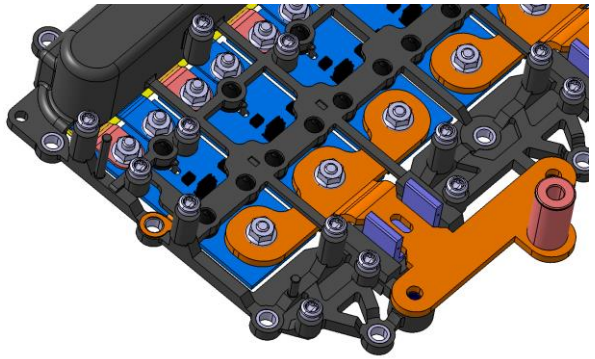
DC Busbars

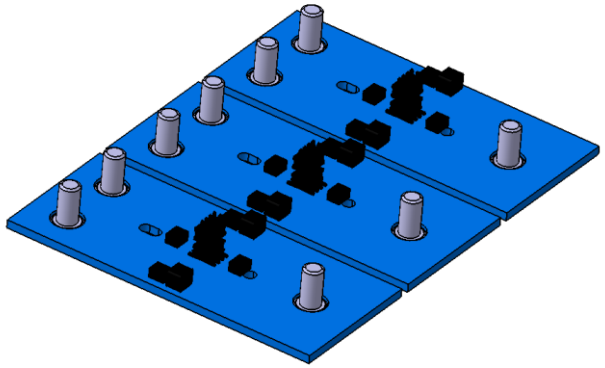
AC Busbars

Press In Thread

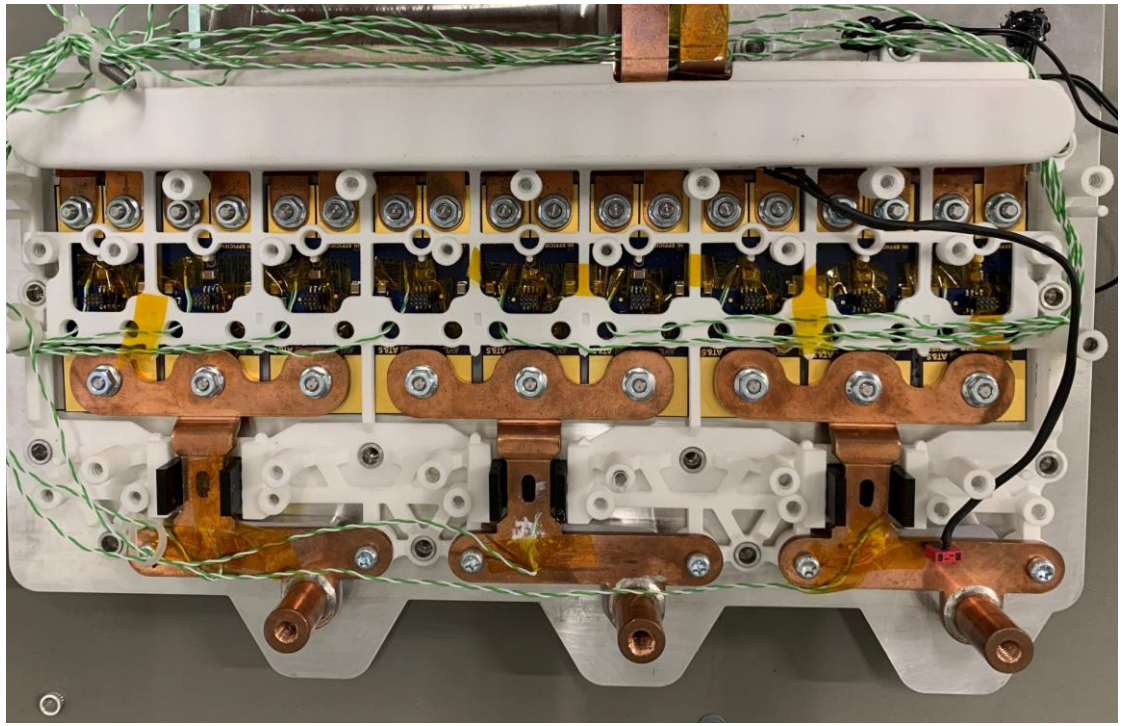
Bottom View







Assembly of the Power Modules in the Inverter



End of Presentation – www.HiEFFICIENT.eu