HI EFFICIENT

WIDE-BANDGAP TECHNOLOGIES FOR TOMORROW'S HIGHLY EFFICIENT

AND RELIABLE AUTOMOTIVE MOBILITY SOLUTIONS

"How to Boost Power Electronics Limits While Ensuring Reliability?"

Jan Albrecht (Technical University Chemnitz) Sajib Chakraborty (Vrije Universiteit Brussel)

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No. 101007281. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Germany, Slovenia, Netherlands, Belgium, Slovakia, France, Italy, and Turkey.







Faculty for Electrical Engineering and Information Technology Center for Micro and Nano Technologies



Center for Micro and Nano Technologies (ZfM) Prof. Dr. Harald Kuhn Dr. Jan Albrecht Dep. Head of Department Micro Materials Center at Fraunhofer ENAS and ZfM Group Leader: Component Reliability







Faculty of Electrical Engineering and Information Technology Center for Micro and Nano Technologies









Smart Systems Campus Chemnitz – Reichenhainer Str.



Buildings of Chemnitz University

Fraunhofer institutes

Start-Ups and companies



MOBI-EPOWERS IN NUMBERS



Power Electronics

Charging Systems Inverters & multi-level converters DC/DC converters & Active Front-End (AFE) Battery Management Systems (BMS)

Electrical Machines

Design and Optimization System Control Performance Assessment

Vehicle Powertrains

Digital Twin Powertrain Codesign Optimization Framework ECO-energy management strategies Fleet Electrification

Smart Green Grid Solutions

Design, Optimization and Sizing of Green assets Energy-Thermal Management and Control system Optimal Charging & V2X (V2G, V2B, V2H, V2D) Strategies

Digital Twin and Reliability

Team Lead: Dr. Sajib Chakraborty

Virtual prototyping and validation of PE converters Virtual vehicles simulation and Fleets management Lifetime testing/ALT testing and RUL estimation



EU funded projects



Members



Research Tracks

Top-Notch Labs

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MAIN CONTACTS



Prof. Dr. Omar Hegazy Omar.Hegazy@vub.be Head of EPOWERS





Part I: Streamlined Power Electronics Optimization with "Design for Reliability (DfR)"

The Critical Role of "Design for Reliability" in the Early Design Phase

Reported Reliability issues

- Σ 1.9 million cars recalled to fix batteries overheating [1]
- **Σ** Nearly 130K+ EVs recalled for overheating of processors [2]
- Σ Over 120K+ EV/PHEVs were recalled due to a risk fire by a Capacitor [3].
- Σ 400k+ cars recalled due to unexplained overheating of inverter [4]

Significances of poor Reliability

ΣRevenue loss

- Σ Customer dissatisfaction
- Σ Long delivery delay
- Σ Disrupted services

A Consequence of Semiconductor Failures in a DC Fast Charger

Consumer Reports: Electric vehicles less reliable, on average, than conventional cars and trucks



→ Trend from 8000 hours to 100,000 hours of operation time, due to EV grid connection

Source:



^{1. &}lt;u>https://www.cnbc.com/2023/11/02/toyota-recalls-nearly-1point9-million-rav4s-to-fix-batteries-that-can-move-during-hard-turns-and-cause-a-fire.html</u>

https://www.theverge.com/2022/5/10/23065987/tesla-recall-130000-vehicles-fix-touchscreen-issues-caused-overheating-cpu-amd-ryzer

^{3. &}lt;u>https://movemnt.net/why-have-270000-vehicles-been-recalled-in-past-week/</u>

https://www.latimes.com/local/california/la-fi-prius-overheat-inverter-defect-20190414-story.html



Improvement considering "Streamlined Design for Reliability (DfR) Approach"



Source: Design for reliability and robustness tool platform for power electronic systems



Methodology of Streamlined Optimization with "Design for Reliability (DfR)"



The <u>streamlined DfR framework</u> functions as follows:

- The DfR framework evaluates DUT lifetime based on electro-thermal stress responses from optimized designed prototypes
- If the target lifetime isn't met, it provides feedback to the optimizer for re-optimization based on a reliability scorecard
- This ensures optimal component sizing, reduces over-engineering, minimizes environmental impact, and extends component life



HIEFFICIENT Use Case Definition & Specification







T-Type Active Front End

Dual Active Bridge

Description	Values
Input voltage	3ph 230V
Output voltage	200V to 1000V
Output power	30kW @ 40°C
Max DC output current	30kW/350V=86A
Bidirectional	Yes

Use Case Lifetime Target:

1. Efficiency:

- 97% @ (30kW 40°C 350V and 1000V)
- 98.5% efficiency AFE
- 98.5% efficiency DAB
- 2. System Lifetime > 150 thousand hours (MTBF)



Multi-objective Design and Optimization



DC-Link Capacitor (x4)			
PARAMETER	VALUE		
PART NO	'MKP1848C66012JY5'		
CAPACITANCE	60uF		
PARALLEL	1		
LIFETIME	151kHr		

1600

1400

AFE Side LCL Filter Inductor

PARAMETER	VALUE	
INDUCTANCE	65 uH	
CORE SHAPE (PART NO)	906	
CORE MATERIAL	Edge- 19u	
NUMBER OF TURNS	49	
COPPER AREA	9 mm^2	

Grid Side LCL Filter Inductor

PARAMETER	VALUE	
INDUCTANCE	19.5 uH	
CORE SHAPE (PART NO)	906	
CORE MATERIAL	Edge- 19u	
NUMBER OF TURNS	27	
COPPER AREA	9 mm^2	

1000

1200



Charging-Profile Definition



Charging characteristics
 ✓ Fast, slow, driving or not? Preconditioned or not?

Condition	Cabinet Temperature (°C)	Charging cycle description	
Critical mission Drofile (CNAD)		- 12 minutes CC (30 kW)	
	45	- 20 minutes of constant discharge (30 kW)	
		- 12 minutes CC (30 kW)	
Adjusted Mission Profile (AMP)	45	- 5 minutes CV	
		- 10 minutes of constant discharge (30 kW)	
		- 12 minutes CC (68% load)	
Heliox defined Mission Profile (HMP)	45	- 5 minutes CV	
		 - 20 minutes of constant discharge (68% load) 	



Charging Profile Based Multi-X Simulation



Multi-X Simulation Analysis: Based on detailed Electro-thermal simulation we found that the **Mean Junction Temperature** (Tjmean) and **Junction temperature swings** (Δ Tj) are ~ **2.5 times** more aggressive in the **T-type AFE** compared to **DAB** throughout all operating conditions. **Results** \rightarrow Hence the Critical DUT is **T-type AFE**

8 October 2024

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Mission Profile to Thermal Stress Translation





Lifetime Assessment Framework



Source: S. Chakraborty et al., "Real-Life Mission Profile-Oriented Lifetime Estimation of a SiC Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 5, pp. 5142-5167



Lifetime Model Parameters

	Parameters	Value	Unit	Experimental condition
	A	3.4368×10^{14}	-	
	α	-4.983	-	$64K \le \Delta T_j \le 113K$
	β_1	-9.012×10^{-3}	-	$0.19 \le ar \le 0.42$
	β_0	-1.942	-	$0.19 \le ar \le 0.42$
SiC	С	1.434	-	$0.07s \le t_{ON} \le 63s$
MOSFET	γ	-1.208	-	
	f diode	0.6204	-	
	ar	0.31	-	
	E_a	0.06606	eV	$32.5^{\circ}C \leq T_{jm} \leq 122^{\circ}C$
	k _b	8.61733×10^{-5}	eV/K	-
DC Link	L _f	5,000	hr	@ 85 ⁰ C
Capacitor	T_f	358	К	-
	V _f	1200	V	DC

According to © 2018 Cree, Inc. the power cycling reliability performance is comparable between discrete SiC and Si devices.



Number of field hours for CREE SiC discrete devices subject to various drain voltages (on the left) and gate voltages (on the right). Drain bias range where avalanche voltage breakdown and gate oxide wear out occurs is far beyond the rated 1,200 V (middle).



Reliability Matrix: target > 150 thousand hour

For lifetime estimation, we consider that the <u>T-Type AFE converter</u> will be subjected to <u>10 same profiles/day</u> during its entire life cycle, which means daily the charger will operate a <u>minimum of 4 hours 30 minutes</u> and <u>a maximum of 6 hours 10 minutes each day</u>. And the ambient temperature will remain the same at <u>45°C facilitated by preconditioning</u> before each charging cycle.

Scenario Condition	Operational cycles/day	MTBF in thousand hours	MTBF in thousand hours With 2% less ΔTj	MTBF in thousand hours With 10% less ΔTj
Critical mission Profile (CMP)	10 cycles Total 6hr 10 min	103 (F)	114 (F)	165 (P)
Adjusted Mission Profile (AMP)	10 cycles Total 4hr 30 min	141 (F)	153 (P)	-
CPO Mission Profile (CpMP)	10 cycles Total 6hr 10 min	380 (P)	-	-

MTBF of the UC4 charging system, P= pass to meet design criteria, F= fail to meet design criteria



Re-optimization to reduce ΔT_j by 10%

The results from the lifetime study show that to achieve the project KPI of 150khr operation time for **CMP**, junction-to-heatsink resistance should be reduced from 0.1 W/K to 0.09 W/K (10% decrease). This decrease can be achieved by a few methods:

- changing the semiconductors
- using different heatsink materials or changing the thermal design
- changing cooling parameters such as flow rate and coolant temperature
- using thermal interface materials with lower thermal resistance





Design Guide To Match Lifetime KPI

Definition	Product Type	Thickness	Thermal Properties
		(mm)	(W / m K)
TIM1	Ceramic	0.635	200
TIM2	Ceramic	0.635	25
TIM3	Silicone Free Thermal Gap Filler	0.5	10
TIM4	Ceramic	2.03	15





CFD simulation results showing overall temperature distribution with TIM1 at 2L/min at extreme condition

Any design choice under the dotted area fulfill the lifetime criteria



Conclusion

• WBG Semiconductors arrived in automotive and charger applications and offer a huge potential for tomorrow's green mobility

- Optimal Design to achieve efficiency and cost is not Enough
- **Design for Reliability** is key for the broad application and needs to be considered already in the **design phase**



Part II: Application of Deep Physical Modelling for Reliable Designs and Condition Monitoring of Power Electronics



Motivation: Product Lifecycle

Typical processes in the product lifecycle





Failure Modes

Failure Cause

In-appropriate design rules and/or material choices, production processes, load condition, harsh environments

Failure Mechanism

Physical, chemical, electrical or other process that results in a failure. It describes how a degradation process preceeds.*

Failure Mode

The effect or manner by which a failure is observed to occur. It is the effect of the failure mechanism.*

Failure Effect

Deviations of (measurable) device parameters during a test run



Alexander Otto, Lifetime modeling of discrete power devices under consideration of superimposed power cycling tests, PHD Thesis, TU Chemnitz

Microscopic cross section after TST2 (800 cycles):





 ε_a^{el} cyclic elastic strain amplitude

 N_f

 σ'_f

 ε_a^{pl}

10¹¹

10¹²

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Bond Wire

 $\Delta \varepsilon_{total}$

20K

Basquin zone

(low ∆T, elastic dominant)

10¹⁰

Foot

60K

10

35K

10⁸

N_f (cycles)

30K

10⁹

25K



UC2 Multidrive e-powertrain





Framework: FEM

Load Case Scenario Standard test profile Mission profile









Electric-Thermal Simulation - Electrostatic analysis



Global Thermal-Mechanical Simulation - Mechanical behaviour for validation (warpage)



Local Thermal-Mechanical Simulation
- Mechanical stress and strain

Creating virtual training data by means of validated electro-thermo-mechanical simulation models



Framework: Surrogate Model

Virtual training





Framework: Health State Assessment

Verified Model



Health State Assessment

orig_T 240: prediction and original over time - zoom: middle

Surrogate Model: T



std: 2.6824 %

14 units, 1 layer, 150 epochs training

 $I \Rightarrow T$

 $seq_{len} = 240$





T. Horn et. al, influence of reducing the load level of master process of the second level of the second l No. 1. 2024 https://doi.org/10.36001/phme.2024.v8i1.3979







8 October 2024

J. Albrecht, T. Horn, S. Habenicht and S. Rzepka, "Mission Profile related Design for Reliability for Power Electronics based on Finite Element Simulation," 2023 IEEE 25th Electronics Packaging Technology Conference (EPTC), Singapore, 2023, pp. 722-726, doi: Confidential / Public 10.1109/EPTC59621.2023.10457766. life of a TO220 analyzed with a surrogate model", PHM Society European Conference. Vol. 8. No. 1. 2024, <u>https://doi.org/10.36001/phme.2024.v8i1.3979</u>



State of Health and Life-Time Estimation



Lifetime extension by reducing the level of stress based on an a priori assessment of the state of health



Applications

LSTM model is running on a microcontroller



LSTM model is implemented in a .fmu



- Implementation possible in system simulations
- Every program which can read .fmu can use the LSTM model and the SoH calculation



Conclusion and Outlook Part II

- Reduction of the computation time for 1 WLTP (1800s) from 2x ~1d to 2x ~10s (for TO220)
- Reduction of the computation time for 1 WLTP (1800s) from 3x ~1w to 2x ~12s (for FS03)
- The framework can also be applied to other components and modules
- The calculation is significantly faster than real time
 → It is possible to perform load variation calculations in time
- Application:
 - Condition Monitoring: implementation on microcontroller
 - System simulation: implementation in a .fmu (also .exe possible)

To be done:

- Application to other failure modes
- Including feedback loops in order to cover influence of increasing failure
- Reduction of the required data points in the training data while maintaining good prediction quality
- Comparison of different network structures with regard to prediction quality
- Covering multiple failure modes within one model





Picture source: https://de.m.wikipedia.org/wiki/Datei:Under_construction_icon-yellow.svg



Conclusion

- WBG Semiconductors arrived in automotive and charger applications and offer a huge potential for tomorrow's green mobility
- Optimal Design to achieve efficiency and cost is not Enough
- Design for Reliability is key for the broad application and needs to be considered already in the design phase
- Another key is the trustworthiness of power electronics, which can be achieved through DfR and condition monitoring

HiEFFICIENT contributed with novel frameworks for Design for Reliability (DfR) and Condition Monitoring of power devices/systems



End of Presentation – www.HiEFFICIENT.eu