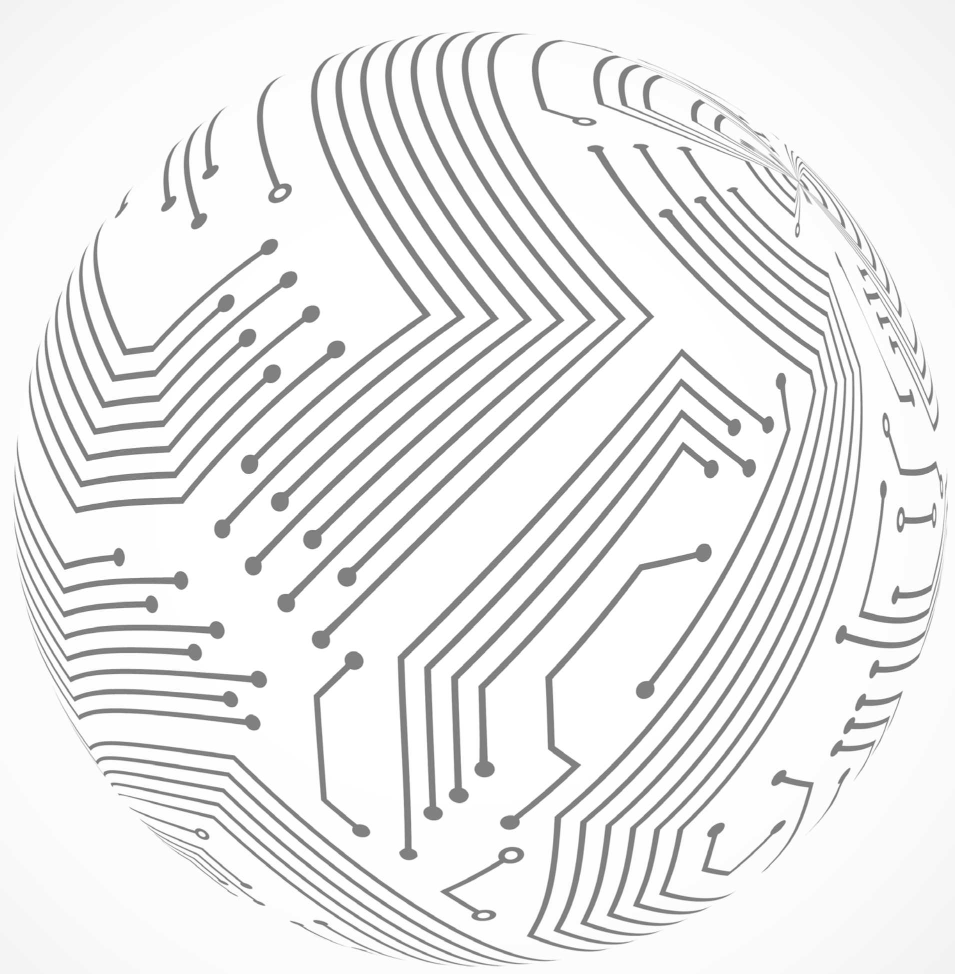
EVALUATION REPORT



DELIVERABLE 1.6

Highly EFFICIENT and reliable electric drivetrains
based on modular, intelligent and highly integrated
wide band gap power electronics modules

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PREFACE

This booklet summarises the main outcomes of the HiEFFICIENT research project – Highly EFFICIENT and reliable electric drivetrains based on modular, intelligent and highly integrated wide-bandgap power electronics modules – funded by the Chips (formerly ECSEL) Joint Undertaking (Call 2020).

Wide-bandgap (WBG) semiconductors are crucial for the advancement of the next generation of electric vehicles. Their superior performance over Silicon semiconductors facilitates a quicker shift towards sustainable future mobility. The HiEFFICIENT project focused on enhancing the power density and reliability of WBG semiconductor-based power electronic solutions for automotive applications, including electrified vehicles and associated charging infrastructure. WBG materials like Silicon Carbide (SiC) and Gallium Nitride (GaN) offer advantages in switching performance, operating temperatures, and power densities, reducing energy losses, size, and weight of power electronics compared to widely used Silicon semiconductors.

The HiEFFICIENT project addressed various automotive applications through six industrial use cases, which included inverters for electric vehicles at different power levels, power electronic converters for on-/off-board charging systems, and power electronics for testing systems for electrified vehicles. A Prognostics Health Management and Reliability Framework was also developed across all use cases to ensure high reliability in respective applications.

After three and a half years, almost all goals have been successfully met. This document presents the achieved results and outlines the benefits for end users.

Lastly, a heartfelt "Thank You" to all project partners for their excellent collaboration throughout the project's duration, as well as to all work package and use case leaders for managing the various work streams and ensuring the project's success.

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We would also like to thank our Project Officer Anton Chichkov, who guided us very well through the project and our reviewers, Sara Giordani and Thomas Harder, for giving valuable input to our project work, helping us to improve the project outcomes.

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Key Facts

START
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COORDINATOR
AVL List GmbH

CONSORTIUM
31 Partners

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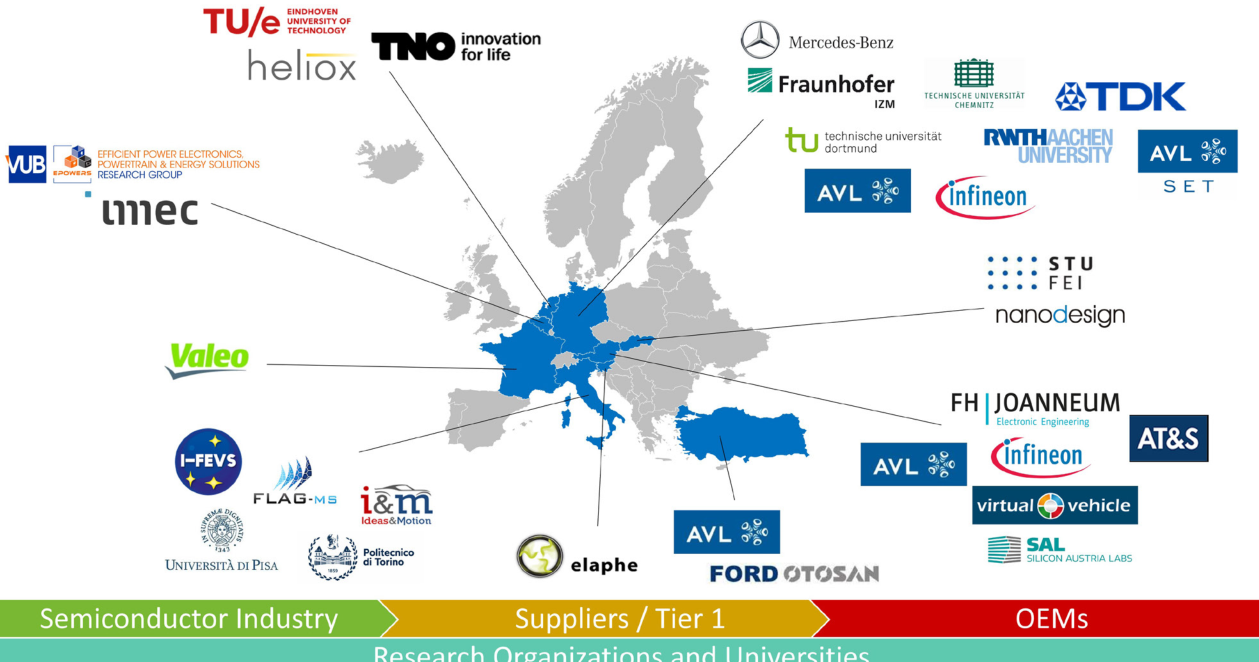
INTRODUCTION

THE PROJECT

The HiEFFICIENT project was initiated in 2021 as a continuation of the HiPERFORM project, which pioneered the use of wide-bandgap (WBG) technologies in electronic power circuits for electrified vehicles and charging infrastructures. Building on its results and insights, the HiEFFICIENT project aims to enhance integration and reduce volume at all levels, from die to system level. It also focuses on improving efficiency and extending lifespan through advanced sensing and control technologies.
With a holistic approach, 31 consortium partners from 9 different countries represent the entire supply chain, ranging from semiconductor up to vehicle manufacturers.

The project addressed developments along the whole value chain by

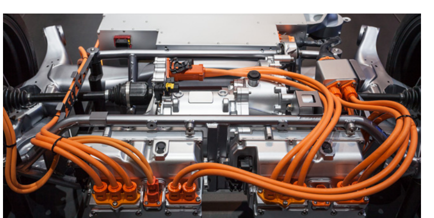
- designing new power devices and switches
- integrating power devices and switches into sub-systems and
- evaluating the newly developed devices on system level in six industrial use cases and more than 10 technology demonstrators.



The industrial use cases included the deployment of WBG power devices in various EV applications such as traction inverters with different power levels, both off-board and on-board charging solutions, and modular power electronics for electrified vehicle testing systems. The specific use cases and their respective leaders are detailed below:

UC1 - ELECTRIFICATION TEST SYSTEMS (AVL List GmbH)
Development of highly compact and reliable test and emulation systems for electric components in electric vehicles using latest SiC and GaN technology.

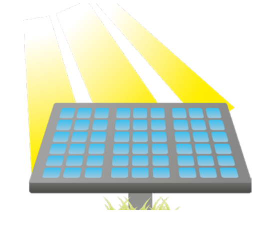
UC2 - E-POWERTRAIN INVERTERS (Ideas & Motion)
Development of two traction inverters, having a focus on fail safe multi-drive powertrain application and on highly integrated powertrain inverter, using power electronics embedding technologies.



UC3 - HIGH POWER 48 V DC/AC INVERTER
(AVL Software and Functions GmbH)
Investigation of the benefits of a highly compact 48 V inverter for use in long-haul heavy duty vehicles. Focus is on the package density and improved reliability.

UC4 - MULTI-USE DC CHARGER (Heliox Energy BV)
Development of bidirectional, flexible multi-output off-board charger, which aims to accommodate different charging needs for different e-mobility devices.

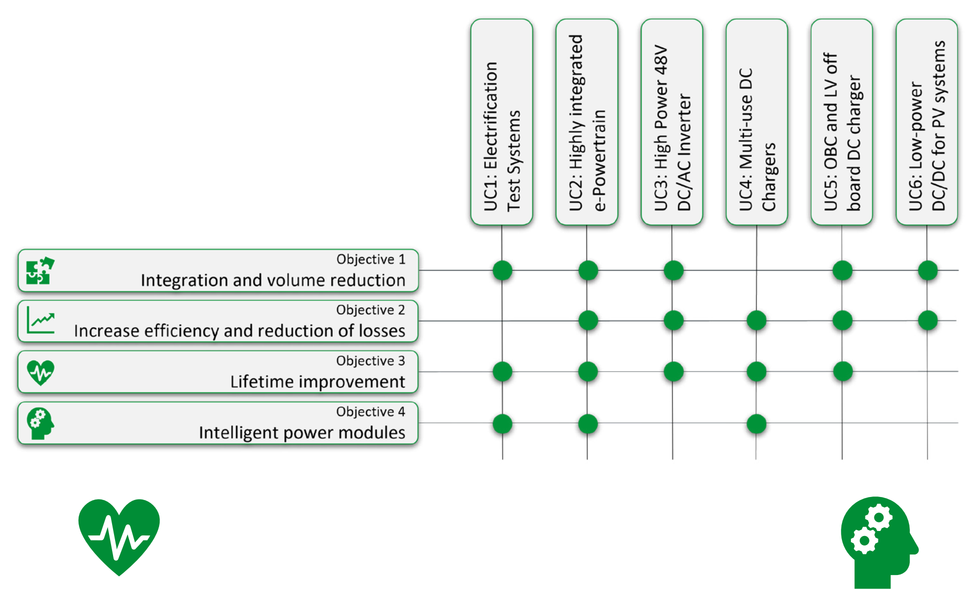
UC5 - ON-BOARD CHARGERS (Vrije Universiteit Brussel)
Demonstration of different power electronic converters for on-board chargers, featuring a more compact system, high efficiency, high power density and integration with other automotive subsystems.

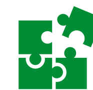


UC6 – MODULAR LOW-POWER DC/DC CONVERTER FOR LOW-POWER PV SYSTEMS
(TU Eindhoven)
Development of DC/DC converter for photovoltaic (PV) applications and benchmarking latest 100 V GaN devices developed in HiEFFICIENT.

PROJECT OBJECTIVES

In the HiEFFICIENT project, significant progress was made towards ambitious objectives improving power electronic efficiency, increasing power density and lifetime of power electronics. This was enabled by developing new GaN devices, demonstrating a 650 V GaN System-on-Chip half-bridge device on one single piece of semiconductor as well as new integration technologies like power electronics embedding in the printed circuit board. Various demonstrators showcased these achievements, each contributing to specific goals.





OBJECTIVE 1: INTEGRATION AND VOLUME REDUCTION

HiEFFICIENT started with the vision to demonstrate the potentials and limitations of integration technologies at various levels, be it at on component (e.g., System-on-Chip, System-in-Package), subsystem (e.g., embedding power electronics components in printed circuit boards) and system level (e.g. on-board-charger and DC/DC converter integration) to achieve a significant volume reduction of up to 40%. First, HiEFFICIENT partners succeeded in developing most compact 100 V GaN System-in-Package devices, having a half-bridge configuration, being about 15% more compact than comparable state of the art solutions at this point in time (12/2022). Some passives could be integrated additionally, which enabled excellent switching behaviour without increasing the volume. Furthermore, first time a 650 V System-on-Chip half-bridge device on one single piece of semiconductor has been developed, and this is still unique for today's available devices. The expectation for the future is, that full SoC integration will lead to better controllable parasitic inductances, which will decrease ringing issues and overshoots. Another leap forward was made with embedding power electronics components in printed circuit boards. This led to a volume reduction of up to 19% compared to SMD based solutions. Additionally, the overall size of an embedded half-bridge SiC module compared to a classic power module was reduced by 30% in area and 50% in volume. On system level, significant advances have been made by driving wide-bandgap devices towards today's limits. So, a power density increase of a power converter by a factor of 2 compared to the baseline has been achieved. Furthermore, an OBC with more than 7 kW/l is demonstrated, outperforming the SOTA of 4 kW/l by a factor of 1.75, relating to around 40% volume reduction. All in all, the set objective was entirely achieved.

OBJECTIVE 2: INCREASE EFFICIENCY AND REDUCTION OF LOSSES

When developing power electronics, efficiency and reduction of losses is key to increase driving ranges and decrease total costs of ownership of future electric vehicles. Hence, almost all use cases in this project had a focus on increasing efficiency and reducing losses in the respective applications. Therefore, efficiencies greater than 98% and 50% reduction of losses were targeted.

One key focus of the project was to enhance loop inductance through embedding technologies and advanced packaging, thereby minimizing parasitic losses and improving efficiency. The prototypes developed demonstrated notable improvements, achieving up to 50% better performance, depending on the specific package or module being compared. The measured stray inductances decreased to as low as 3.4 nH, compared to similar state-of-the-art power modules that measure 8 nH. These improvements contributed to the design of highly efficient converter systems, achieving peak efficiencies up to 98%.

Other development aspects have been on the optimization of low-level control strategies and active gate driver (AGD) networks to improve efficiency. Project partners could demonstrate the benefit of Discontinuous Pulse Width Modulation (DPWM) compared to standard Space Vector PWM (SVPWM) showing up to 3% efficiency improvement in low speed and low torque regions of an inverter application. In case of AGDs 15-20% lower turn-on losses have been achieved.

OBEJCTIVE 3: LIFETIME IMPROVEMENT

The HiEFFICIENT project achieved significant advancements in Reliability and Prognostic Health Management (PHM) for power electronic converters, targeting a lifetime enhancement of 20%. The project investigated lifetime enhancements from component to system level. At component level, efforts have concentrated on improvements in chip packaging, i.e., novel chip embedding concepts in the PCB. Therefore, advanced multi-physics simulations have been conducted, including complex electro-thermal and thermo-mechanical analyses. The developed solutions showed significant improvements with respect to loop inductance (up to two times), switching overshoots (up to 15%) and switching speed (up to 30%), consequently leading to higher efficiencies while ensuring higher margins for junction temperatures to maximize component lifetime. Furthermore, it could be proven that a significant increase in robustness is possible based on this packaging concept (50 times longer lifetime). Another focus was on data-driven and hybrid PHM methods. By analysing key packaging related failures such as bond wire lift-off and die attach degradation, newly developed methods have been integrated in innovative control algorithms and real-time monitoring systems for predictive maintenance, meeting reliability targets. Additionally, Design for Reliability concepts have been followed, to reach for a multi-use DC charger Mean Time Between Failures (MTBF) of over 150,000 hours, representing a 50% improvement in MTBF. Finally, a novel power electronics lifetime testing setup has been developed, confirming the feasibility to assess series failure rates of power electronic components, e.g., inverters. Overall, HiEFFICIENT successfully enhanced power electronics reliability, directly addressing critical technology bricks for improved thermal management, failure prevention, and extended system lifetimes.

OBEJCTIVE 4: INTELLIGENT POWER MODULES

WBG semiconductors enable applications and systems with increased power density, faster switching, and higher operating temperatures compared to Silicon semiconductors. Accelerated switching has great potential to reduce losses, but it often comes with increased current overshoot and parasitic ringing. Therefore, different concepts to enhance the performance of the power electronics have been investigated. They showed significant advances for future applications, and a few examples are highlighted in the following. One approach followed was the development of an active gate driver (AGD) network to achieve a faster turn-on switching transient and to reduce the turn-on switching losses without increasing the parasitic ringing and current overshoots. The developed AGD allows simple integration into existing designs, specifically not requiring any modifications of the controller. Measurement results demonstrate that 15-20% lower turn-on losses can be achieved without increasing parasitic ringing and current overshoots. Further an adaptive gate driver has been developed to control the gate voltage actively. This enables the control of the junction temperature of SiC MOSFETs by manipulating the conduction losses and hence, reduces the thermal cycling of the power switches. Lastly, a generative adversarial network temperature-dependent thermal model has been developed, to estimate SiC die junction temperatures. Thereby a temperature sensing bandwidth of 20 Hz has been achieved. This is a significant advance compared to traditional systems, which often operate below 10 Hz. This higher bandwidth enables more accurate and faster thermal monitoring of the power semiconductors.

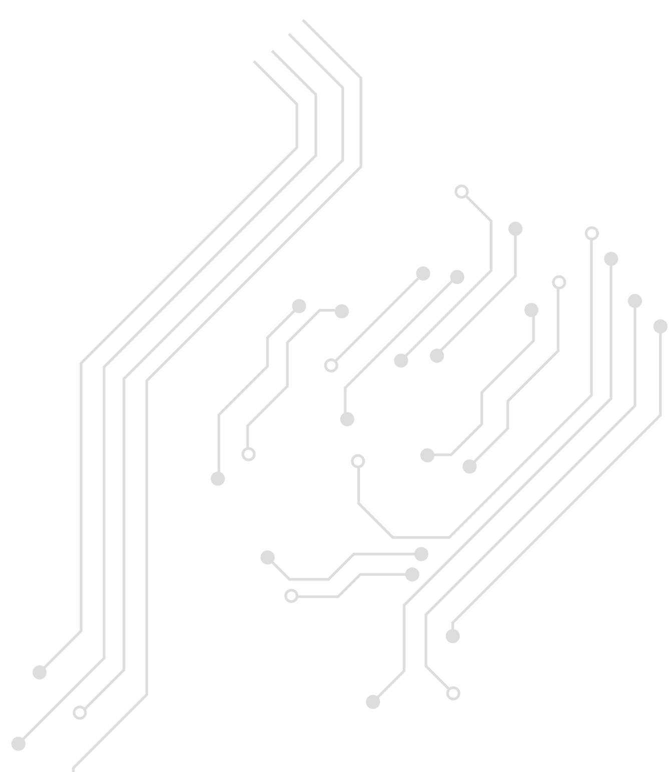
FIRST GAN SIP AND SOC DEVICES OUT OF EUROPE

INTRODUCTION

Gallium Nitride (GaN) System-on-Chip (SoC) and System-in-Package (SiP) solutions represent a significant advancement in power electronics, combining the high efficiency and fast switching capabilities of GaN technology with the integration benefits of SoC and SiP designs. These solutions integrate multiple functions, such as power control (i.e., gate driving circuitry) including possible sensing functionality (i.e., current and temperature sensing) and power conversion into a single chip, reducing the overall system size and complexity. In this project, two different voltage ranges were targeted in case of SoC designs: 100 V and 650 V, using imec's technologies. The 100 V SoC in HiEFFICIENT was designed and developed in the baseline GaN-IC technology on GaN-on-SOI substrates; whereas the 650 V SoCs were developed using the baseline 650 V baseline GaN-IC technology on GaN-on-poly-AlN (engineered) substrates. Two learning cycles were designed, yet only the SoCs of learning cycle one went to the embedding processing and to the UCs. The second learning cycle SoCs were tested by imec for their functionality only, since advanced packaging allowing for power conversion was not available within the time frame of HiEFFICIENT.
Secondly, SiP devices by Infineon were developed, integrating in a half-bridge laminate package module 2x 100 V 3 mOhm CoolGaN HEMTs, a half-bridge driver with integrated bootstrap diode, high-frequency bypass capacitors, gate resistors, and a bootstrap capacitor.

PROGRESS BEYOND STATE OF THE ART

The current landscape of GaN technology features mainly System-in-Package (SiP) solutions and just a few System-on-Chip (SoC) solutions from various leading companies. Navitas Semiconductor offers GaNFast™ power ICs, which are highly integrated SiP solutions combining GaN power FETs with drive, control, and protection circuits within a single package. Efficient Power Conversion (EPC) provides true SoC solutions with their eGaN® ICs, such as the EPC2152, which integrates GaN FETs with drivers and level shifters on a single die, targeting 100 V applications. Innoscience provides highly integrated SiP solutions like the ISG3201, which integrates two 100 V 3.2 mOhm e-mode GaN HEMTs with driver circuitry, but it is not a true SoC. Vanguard International Semiconductor (VIS) and ST Microelectronics offer highly integrated GaN solutions, but these are typically SiP rather than true SoC. VIS's 650 V GaN-on-QST technology and ST's MasterGaN family combine GaN transistors with drivers and protection circuits within a single package, suitable for high-power efficiency applications.
Overall, while true GaN SoC solutions are emerging, many companies still rely on SiP technology to achieve high levels of integration and performance across various voltage classes and applications.
In HiEFFICIENT, imec demonstrated true monolithic integration of a full half-bridge and gate driving circuitry and this for both 100 V and 650 V. The size of the power switches on these SoCs had to be limited in order not to end up with too large footprints, yet competitive on-resistance values could be reached.
Furthermore, Infineon demonstrated most compact 100 V GaN System-in-Package devices, having a half-bridge configuration, being about 15% more compact than comparable state of the art solutions worldwide.



TANGIBLE RESULTS

During the HiEFFICIENT project, two learning cycles were completed for each voltage range up to the functional measurements of the SoCs. This results in 4 different full reticle designs that were drawn and used in several device lots. Each of these designs contained several SoC variants changing in complexity ranging from simple half-bridge (two power switches without any additional circuitry) to half-bridges with low-side and high-side gate drivers, level shifter, low-side and high-side temperature sensors, protection diode-connected HEMTs at the terminals, pull-down resistors, and low-side and high-side current sensors. An example of such an advanced half-bridge with integrated circuitry is shown in Fig. 1.

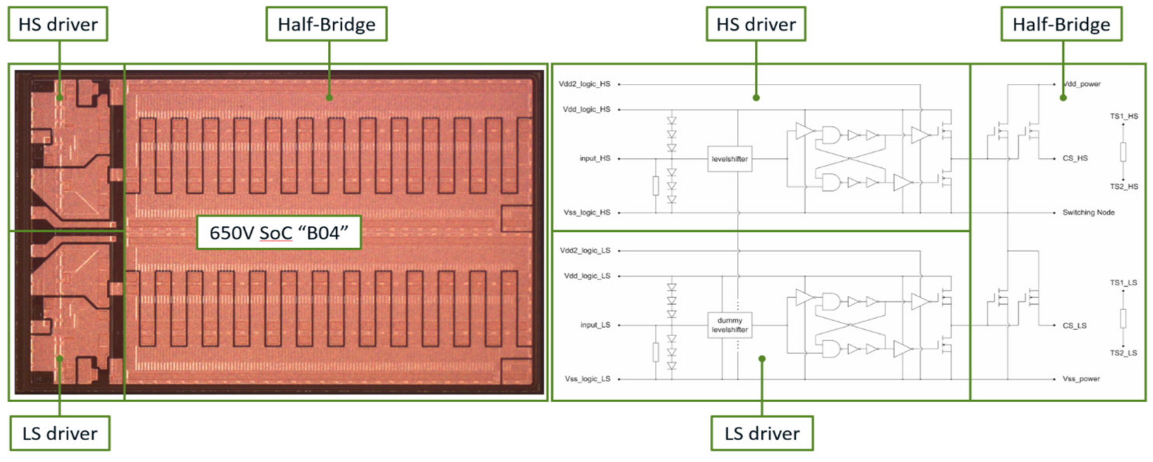
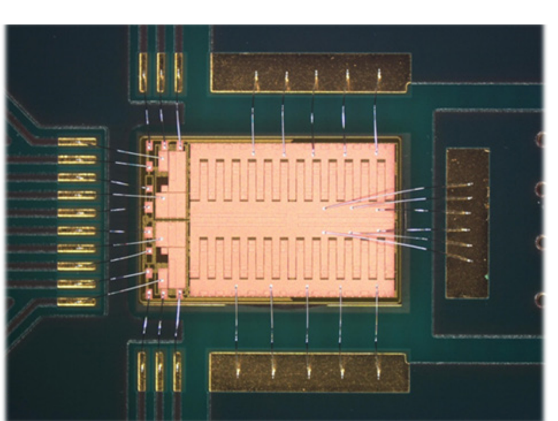


Fig. 1 Image of one of the GaN 650 V SoC variants (left) and the block diagram (right)

Functional test measurements were carried out by imec as seen in Fig. 2. Several SoCs (both for 100 V and 650 V and from both learning cycles) were already tested and proven to be functional. Of course, these functionality tests are limited in current (and voltage for the 650 V), and switching frequency as the wire bonding of the SoC to the test interposer board is not an ideal power application solution. For the second learning cycle design, the targeted on-resistance values for the power switches on the SoCs were as low as 8 mOhm (100 V SoCs) and 105 mOhm (650 V SoCs), with current levels targeted at 125 A and 16 A, respectively.



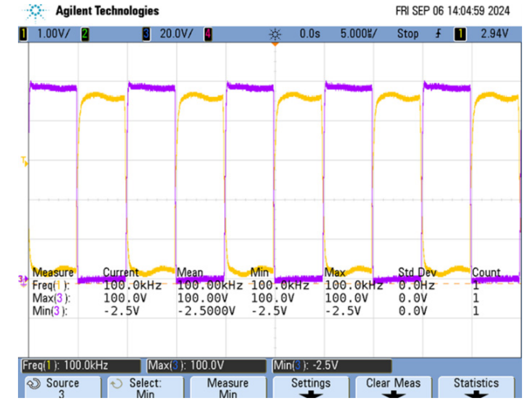


Fig. 2 One of the SoCs wire-bonded towards an interposer board for functionality testing (left). Result of one such functionality test (right)

KEY RESULTS

Infineon has successfully integrated current and temperature sensors within the GaN HEMT device to improve future SoCs which can be integrated in a SiP (for example temperature sense and current sense on a SoC and the driver together with the SoC in a SiP). Thus, enabling protection against over-current peaks, short circuit events, and operations outside the safe operation area. This is crucial as a 3 mOhm transistor which can deliver 400 A during a short circuit. A novel current sensor was developed in the HiEFFICIENT project, while the initially proposed temperature sensor based on 2DEG temperature dependency lacked accuracy. A new Schottky diode temperature sensor was developed, providing high accuracy of +/- 5 degrees Celsius. Finally, demonstrators (cf. Fig. 3 and Fig. 4) of a half-bridge laminate package module are integrating

- 2x 100 V 3 mΩ CoolGaN HEMTs,
- 1x half-bridge driver with integrated bootstrap diode,
- high-frequency bypass capacitors,
- gate resistors, and
- bootstrap capacitor.

The module enabled a solution with all essential passives integrated. Moreover, the solution simplifies the system layout and allow the designer to focus only on the system layout optimization. Consequently, this module reduces the overall system cost and time-to-market.

Preliminary tests have been carried out at Infineon side to verify the basic features of the half-bridge module and the ease-of-use of the module could be verified in application later. Especially the external circuit immunity (Fig. 5) showed an excellent behaviour because of the integrated passives.

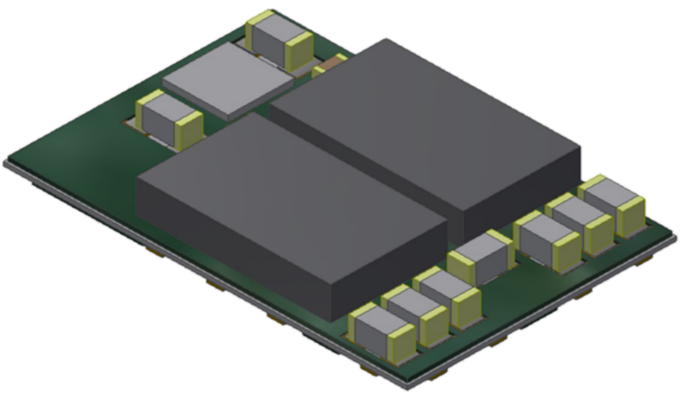


Fig. 3 3D top view inside package of 100 V SiP

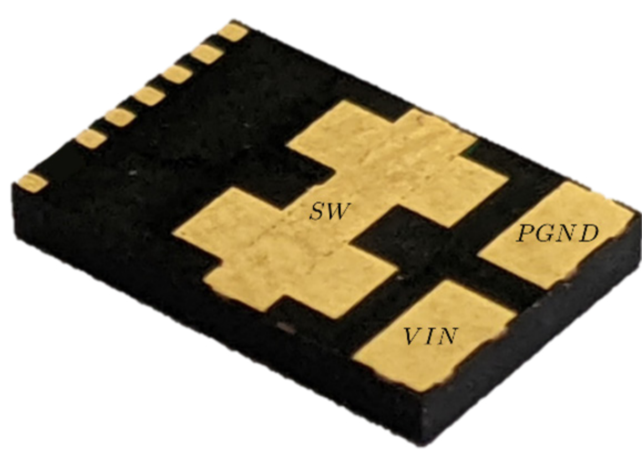


Fig. 4 100 V SiP real-package bottom pad view

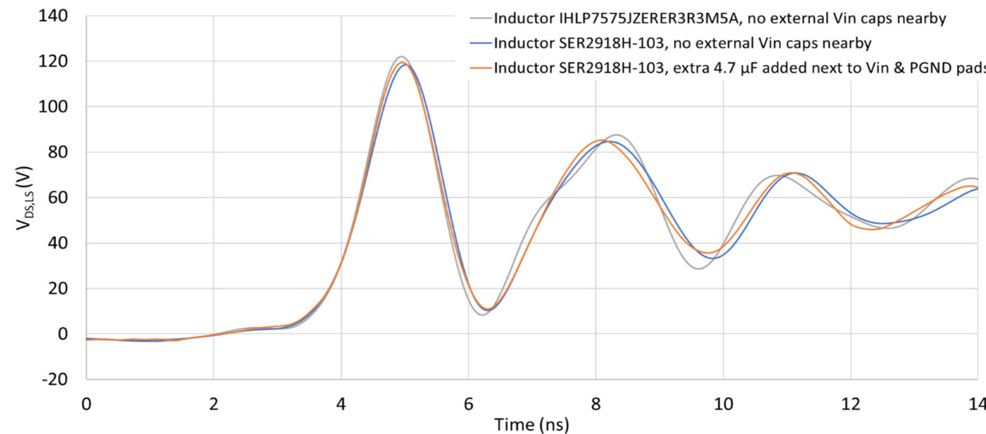


Fig. 5 Preliminary experimental concept validation: external circuit immunity

INTEGRATION METHODOLOGIES AND CONCEPTS FOR HIGH POWER AUTOMOTIVE POWER ELECTRONICS

INTRODUCTION

To improve the efficiency in modern cars on the way to electro mobility, the power density has to increase without limitations on performance and reliability. New module concepts with wide-bandgap semiconductors are the best candidates to face these challenges. First priority is on thermal management and handling of high current. This requests reduction of inductance and switching losses. The implementation of power semiconductors like MOSFETS, IGBTs, or diodes directly into the printed circuit board (PCB) is a very promising approach to fulfil these requirements. AT&S successfully used the expertise with its ECP (Embedded Components Packaging) technology for the implementation of efficient power packages and modules. This made it possible to reduce the space required for power packages by up to 50% with correspondingly higher power density.

PROGRESS BEYOND STATE OF THE ART

In this project AT&S investigated in development of novel integration concepts and interconnect technologies. Therefore, different embedding concepts to realize power modules with integrated discrete SiC devices (UC1), discrete GaN devices (UC3) and the novel GaN SoC devices (UC2b and UC5a) were designed and manufactured.

In relationship to UC1, the build-up of a half-bridge module is visualized in Fig. 1. The heart of this build-up is a so-called PARSEC-power core with the embedded active components. The connection to the component is done by µvia on front side (gate, source) and with direct copper attach on the backside (drain) which is realized by using a galvanic copper process.

Target for the embedded variant was to reduce size and to optimize electrical performance. The module consists of two SiC MOSFETs (1 for high side and 1 for low side), which are integrated with embedding technology into the inner core. The build-up consists of 5 layers. To provide isolation on the back side of the module and improve thermal performance, a thermal prepreg is provided between layer 4 and 5. The front side provides all the functional connections for gate and source sense for high side as well as low side and includes connections for DC+, DC- and switched node.

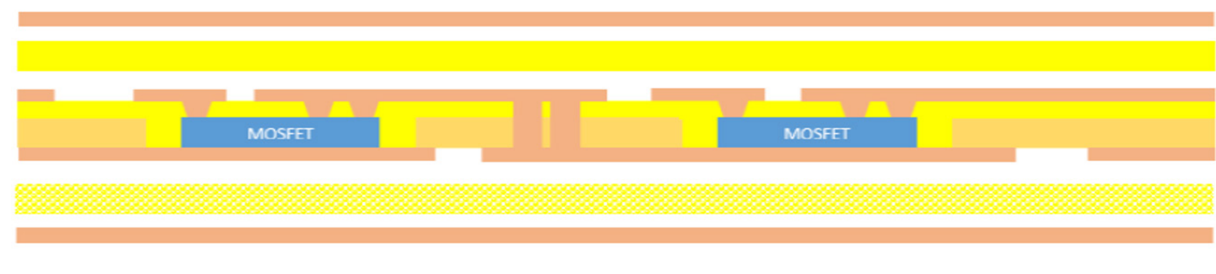


Fig. 1 Block diagram of an embedded half-bridge module

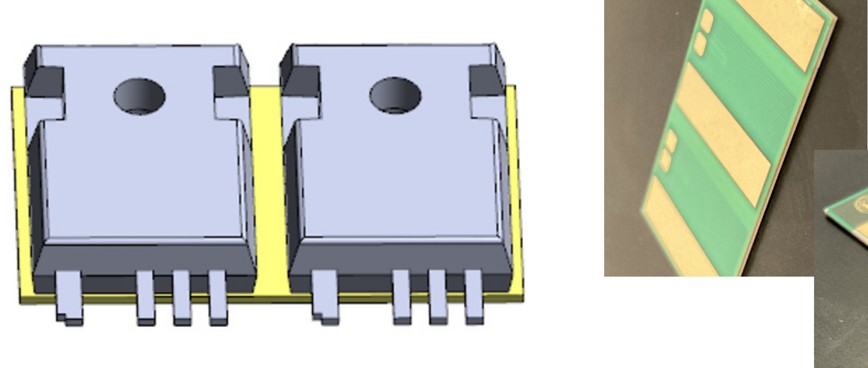


Fig. 2 TO-247 Reference half-bridge left versus embedded module right

As shown in Fig. 2, embedding of SiC bare dies for a half-bridge solution enables a significant reduction of the volume by up to 80%, especially reducing the height to less than 20%. Additionally, an analysis of the loop inductance showed an improvement of 50% for the embedded solution, which enables the possibility of higher switching frequencies.
Furthermore, the development on sinter lamination technology was investigated with different sinter paste materials to be compatible with embedding concepts. In addition, a further objective was to develop embedding and its modifications to enable integration of GaN bare dies realizing higher electrical and thermal performance. Therefore, a GaN based power module using sinter lamination technology for increased current carrying capability was designed and fabricated. As shown in Fig. 3 a PARSEC core and additional a current core are fabricated independently. The PARSEC core consists of two GaN dies in parallel for high side and for low side, the current core is a conventional 6-layer PCB. After fabrication of the 2 cores, the interconnection between them is then realized by copper depots which are sintered during the lamination process (sinter lamination) and, in a last step to provide isolation and increased thermal performance, a thermal prepreg is used on the backside of the module. The size of one half-bridge module is l×w×t = 67×29×1.73 mm.

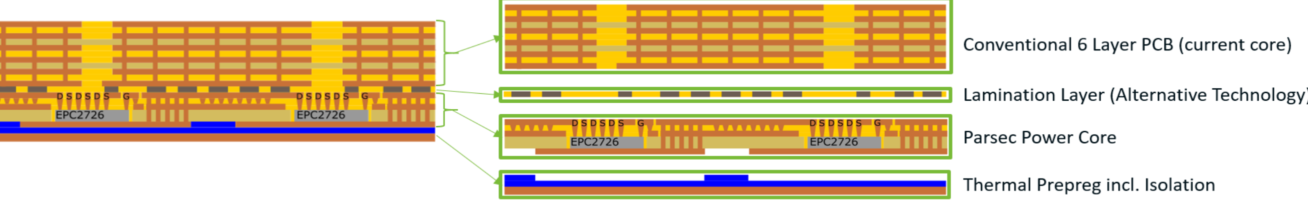


Fig. 3 Schematic build-up of the UC3 power module

The sinter lamination is a novel technology developed in this project and implemented to provide the first functional demonstrators. The alternative connection layer improves the current carrying capability as well as the thermal behaviour for the connection of the two cores. Fig. 4 shows the printed Cu-paste during fabrication and Fig. 5 shows a cut of the finished half-bridge module (whole stack-up including the sintered Cu-Depot).

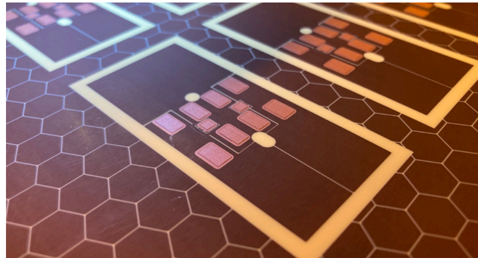


Fig. 4 Printed Cu-paste depots UC3

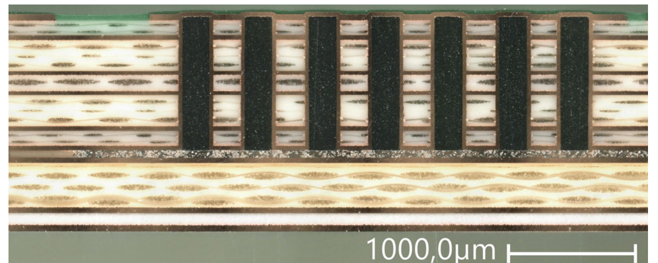


Fig. 5 Full stack-up showing sinter lamination layer including the sintered Cu-paste.

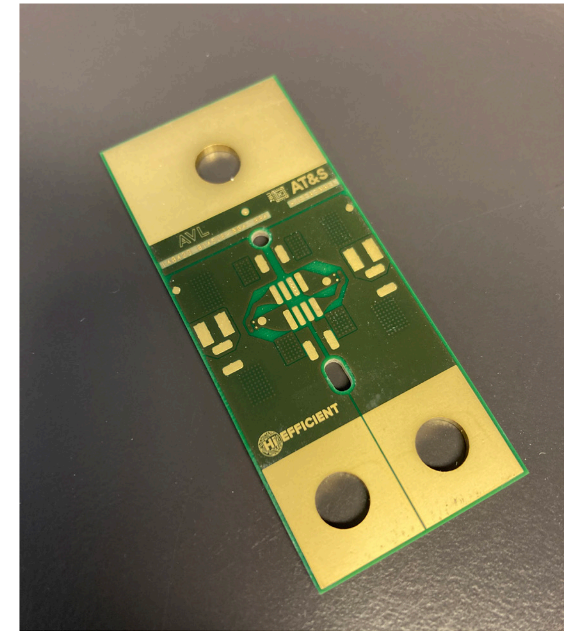


Fig. 6 Half-bridge module

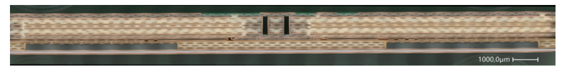


Fig. 7 Cross section of the half-bridge module

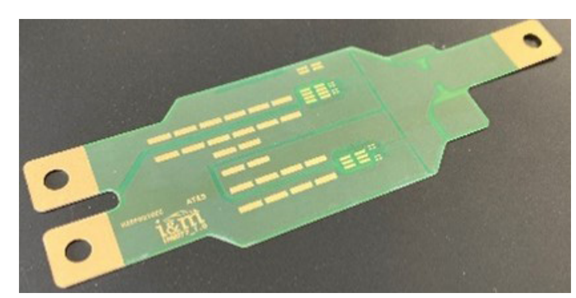


Fig. 8 650 V GaN SoC module

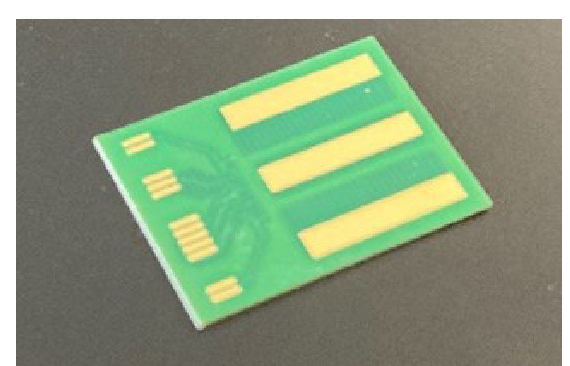
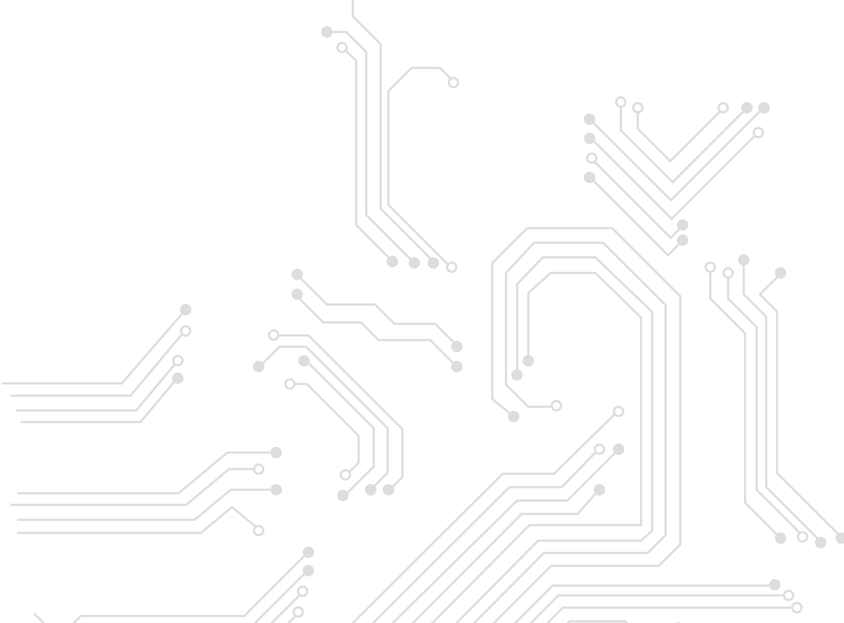


Fig. 9 Single 650 V SoC package

Fig. 6 shows the module after fabrication and Fig. 7 shows the cross section of the low-side of the module. In the cross section, the two parallel low-side GaN HEMTs with front side µVia connection and direct galvanic copper attach on back-side can be seen.
Further, the newly developed 650 V GaN SoC on polyAlN was embedded in the PCB, following two different concepts (Fig. 8, Fig. 9). One concept focused on a power module, having 2 SoCs embedded in parallel by using a PARSEC core and fabricated as an unsymmetrical 3-layer module. The second concept was a single packing of the SoC for further use, comparable to a conventional SMD packaged component.

TANGIBLE RESULTS

By applying embedding technologies significant advances in volume reduction and increasing voltage limits of embedded dies have been demonstrated. In case of the 1200 V SiC half-bridge module, a benchmark compared to the STMicroelectronics SiC Module used in the Tesla Model 3 shows a volume reduction by 75% possible, even if it is rated with lower voltage, but comparable current.
In case of the developed GaN power modules, even a higher volume reduction greater than 90% could be achieved. As a benchmark, a 650 V, 300 A, 3-phase GaN power module (GS-EVM-3PH-650V300A-SM1) was considered for comparison of the 650 V GaN SoC power module developed in HiEFFICIENT.
Besides the volume reduction, also the embedding process could be enhanced by applying sinter lamination techniques using Cu-paste and hence improving the thermal performance of the package.
Another important aspect is a significant enhancement in reliability compared to the conventional packages. This is described in more detail in the key result „Make Reliability and PHM functions visible at the top system level and to the end user".



MAKE RELIABILITY AND PHM FUNCTIONS VISIBLE AT THE TOP SYSTEM LEVEL AND TO THE END USER

INTRODUCTION

Reliability on the one hand and in-depth knowledge of the health status of power electronic devices on the other are crucial to ensure customer acceptance, confidence, and sustainability of tomorrow's power electronics for electric vehicles. Key areas covered in HiEFFICIENT include the development of tests as well as the run of tests for new power modules, the application of Prognostic Health Management (PHM) and multi-physics models for real-time system assessment, and innovative strategies for thermal management and failure analysis. These efforts aim to push the boundaries of current technologies to ensure greater durability and operational efficiency in power electronics systems that are critical to a wide range of industrial and automotive applications. Each demonstrator delivered specific outcomes and technological breakthroughs that contribute to the overall goal of improving system reliability and performance through cutting-edge research and collaboration.

PROGRESS BEYOND STATE OF THE ART

Significant advancements were achieved within HiEFFICIENT, focusing on enhancing the reliability and operational efficiency of power electronics systems through Prognostic Health Management (PHM), condition monitoring, and extensive lifetime testing. Each demonstrator has contributed uniquely to the overarching goal of improving system robustness and performance in industrial and automotive applications.

PHM

Different PHM approaches have been investigated. One comprehensive approach focused on developing a smart multidrive unit that incorporated a PHM method applied to dual inverters. This included the utilization of reliable State of Health (SoH) estimation methods that are both data-driven and based on physics of failure models. The project also introduced first time a hybrid approach that combines data and physics-based methods for assessing the health state of traction inverters, significantly improving the system's fail-safe capabilities and maintenance strategies. Another development targeted a PHM circuit designed to measure Temperature-Sensitive Electrical Parameters (TSEPs) (i.e., on-state voltage, current and on-state resistance), integrating noise removal techniques to ensure accurate data correlation, as shown in Fig. 1. The effectiveness of the circuit in tracking changes in junction temperature showcased its potential as a crucial element in PHM methodologies, enhancing the predictive maintenance capabilities of power electronics systems.

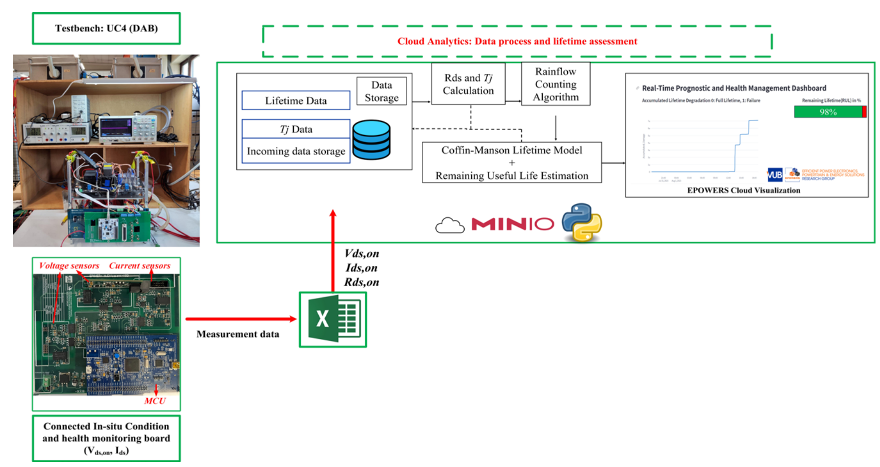


Fig. 1 Cloud-connected in-situ PHM implementation for UC4 including TSEPs measurement hardware and lifetime assessment framework

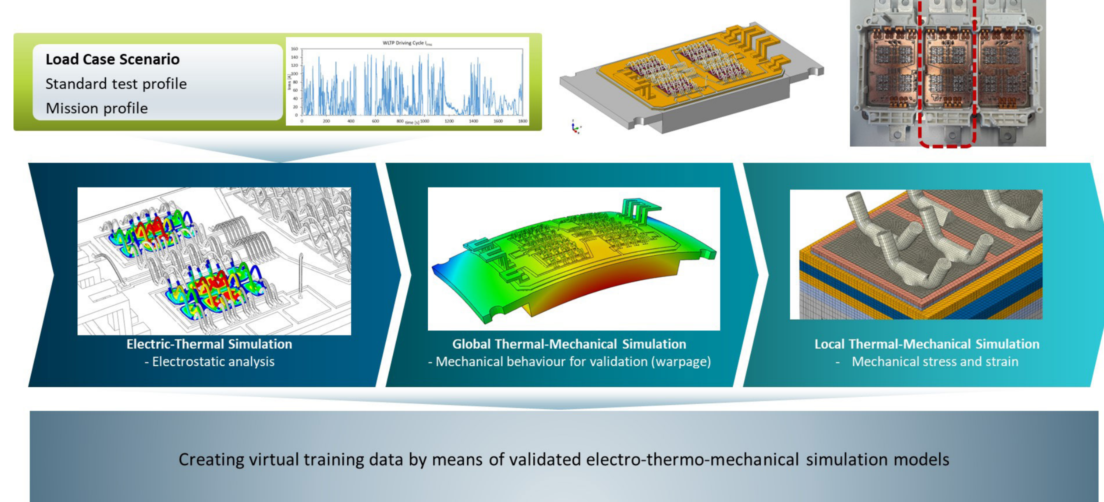


Fig. 2 Surrogate models for electro-thermal-mechanical fatigue assessment

Moreover, another demonstrator focused on assessing the lifetime of GaN switches by developing a PHM to measure the $R_{ds,on}$ before each charging cycle. This approach provided a precise, real-time assessment of the switch's condition, demonstrating a proactive method for predicting component lifespan based on continuous data monitoring.

Condition Monitoring

With respect to condition monitoring, the project partners explored the implementation of condition monitoring in power electronics used in electrification test fields. Techniques such as using gate drivers to maintain constant losses, employing non-invasive temperature measurements to adjust system performance, and applying data-driven methods to assess system health were evaluated. These methods were tested on scaled-down versions of the target platform, validating the concept and demonstrating significant potential for online condition monitoring. This approach, informed by Failure Modes, Mechanisms, and Effects Analysis (FMMEA), sets the stage for enhanced reliability through informed maintenance strategies.

Lifetime Testing

Within HiEFFICIENT, a novel power electronics lifetime testing setup has been developed, confirming the feasibility to assess series failure rates of power electronic components based on mission profile-oriented test data. A streamlined mission-profile-oriented reliability assessment tool was developed that integrates mission profile-oriented measurements with data received from multi-physics models (i.e., electro-thermal and thermo-mechanical), significantly advancing lifetime prediction and failure risk assessment.

Further, the project also placed a strong emphasis on lifetime testing and analysis of power modules, using novel integration methodologies for bare die embedding in a PCB. Thereby, outstanding durability values have been achieved, which are as follows. Various designs of embedded GaN power modules were tested using different GaN dies, specifically 80 V off-the-shelf and imec's 650 V SoC GaN bare dies. The 80 V dies achieved 290,000 cycles, while the 650 V dies reached 490,000 cycles under harsh conditions without failure. Further, 1200 V SiC dies have been embedded in half-bridge configuration in a PCB, which already exceed 500,000 cycles without electrical degradation under controlled load conditions – and still counting. These tests were complemented by detailed mechanical and thermal simulations, as well as physical failure analyses, to understand the stress effects on power modules.

TANGIBLE RESULTS

Overall, the collaborative efforts across the project have led to groundbreaking developments in PHM, condition monitoring, and lifetime testing for wide-bandgap power devices. These advancements not only improve the reliability and performance of power electronics systems but also pave the way for robust predictive maintenance strategies, ensuring long-term sustainability and operational efficiency in a wide range of applications.

Tangible results are amongst others

- newly developed hybrid DD-PoF model,
- surrogate models for electro-thermal-mechanical fatigue for real-time assessment (Fig. 2) as well as according compact models ready for microcontroller implementation,
- PHM circuit to monitor ripple junction temperature ($R_{ds,on}$) to stay within limits,
- Mission-profile oriented reliability assessment tool for optimized design for reliability,
- Active thermal control concepts to minimize thermal cycling,
- Non-invasive junction temperature measurement with high bandwidth,
- Mission profile oriented lifetime test system, and
- Highly reliable packaging concepts exceeding 500,000 power cycles under harsh conditions.

ADVANCED COOLING CONCEPTS FOR HIGHLY INTEGRATED POWER ELECTRONICS

INTRODUCTION

Latest wide-bandgap-based power electronic solutions can efficiently manage large amounts of power. Depending on the application, this can result in very compact designs that require effective heat dissipation. One of the primary challenges for the future miniaturization of electronics is its thermal management. With an increasing number of transistors per square centimeter, the generated heat fluxes will also rise. Forced air convection cooling has reached its limit and no longer satisfies the required thermal loads. Therefore, more sophisticated forced convection liquid and flow boiling cooling are being explored to meet thermal demands in the near future.

In this project, a highly efficient GaN-based amplifier was developed, featuring 48 GaN switches within an area of just 3.4 by 8 cm, releasing up to 1 kW of heat during full operation. This stretches conventional liquid cooling solutions to their limits, necessitating new approaches. Flow boiling in microchannels is a technology capable of absorbing high heat loads with a low flow rate and a compact design. A common issue in microfluidic flow boiling devices is the occurrence of boiling instabilities, which lead to reduced heat transfer and high-pressure fluctuations.

PROGRESS BEYOND STATE OF THE ART

During the project, TNO focused to mitigate the named challenges and developed an advanced microfluidic flow boiling method. Within this project experiments, cooling capacities are achieved in the order of ~250 W/cm^2, which is twice the current state-of-the-art achieved heatflux mentioned in literature. The stable pressure drop over the microfluidic cooler is below 100 mbar, as opposed to the reported several bars to pump the high flow rates through the microfluidic channels operated in literature. Finally, by choosing the appropriate cooling fluid the chip interface temperature is below 90°C, which ensures a junction temperature below 120°C at full operation power. This novel method does not require a complex hierarchical supply and outflow channel, typically seen in literature. To design this high-performance microchannel flow boiling cooling device, proper flow boiling models for microchannels are essential. Within the power electronics system the heat of the chip is first spread by the interposer in which the microfluidic flow boiling method is embedded. This reduces the local heat flux before it is absorbed by the cooling fluid. Existing state-of-the-art models do not take into account the heat spreading (Fig. 1) to predict the temperature of the chip.

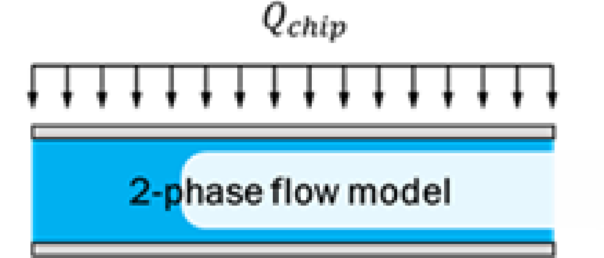


Fig. 1 Schematics of flow a boiling model with fixed uniform heat flux cooled by a two-phase flow

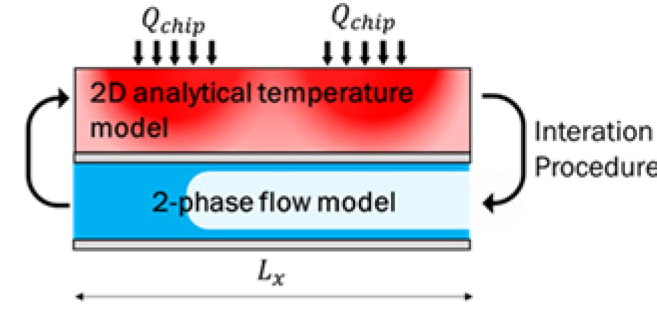
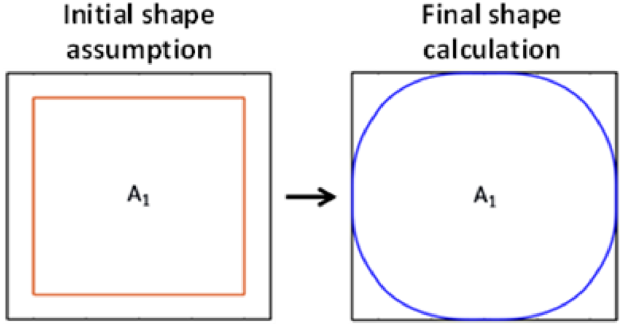


Fig. 2 Schematics of a flow boiling model with a coupled model for heat spreading and flow boiling.

The heat flux is assumed to be constant over the length of the channel. This constant heat flux assumption is inaccurate as the heat flux is a function of both the temperature of the heat spreader and the local boiling state of the fluid. To take the 2D heat spreading into account, a novel model is developed, coupling a 2D temperature model to a micro channel flow boiling model (Fig. 2). This coupled model is used as a design tool to optimize the dimensions of the cooling device. Hot spots or high peak temperatures are prevented.

The TNO model calculates the flow boiling heat transfer coefficient using the thickness of the liquid film. The vapor mass fraction in a section is dependent on the amount of energy inserted in the fluid. The void fraction, however, strongly depends on the shape of the liquid film. An accurate prediction of the film thickness is essential for an accurate heat transfer coefficient prediction. In microchannels the shape of the liquid film is significantly affected by the surface tension. Based on equilibrium models found in literature, TNO developed a numerical method to calculate the equilibrium state of a liquid interface in a rectangular channel. The TNO model is extended with an empirical evaporation resistance and including this numerical method for the film thickness calculation. The effect of this inclusion on the liquid film shape can be seen in Fig 3.



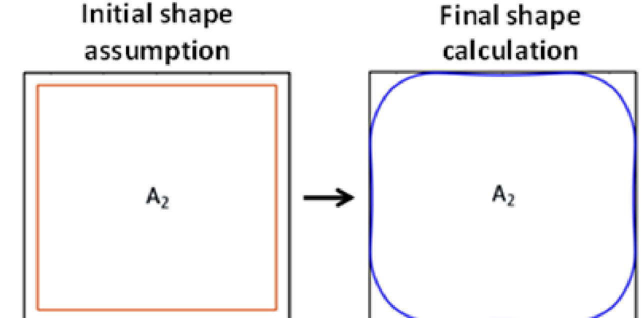
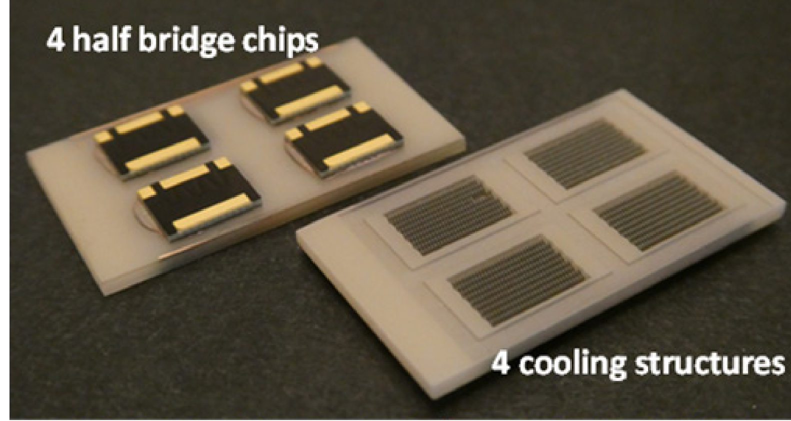


Fig. 3 Surface tension effect on film shape for different void fractions, TNO microfluidic flow boiling model results. Left: void fraction 0.8. Right: void fraction 0.9

The improved modelling led to a microfluidic flow boiling design embedded in the interposer of the power electronics chips, see Fig. 4 left. To validate the models and prove the calculated heated flux, an aluminum mockup setup is designed using heated pillars with the size of the chips, see Fig. 4 right. Therefore, this setup allowed a better-defined thermal boundary condition. The aluminum pillar allows lateral heat conduction with a relatively small temperature gradient, thus approaching the uniform wall temperature at the bottom of the microfluidic flow boiling structure. By means of the two thermocouple holes above each other, the vertical temperature gradient is measured in each pillar. This vertical gradient is used to estimate the wall temperature by linear extrapolation and assuming one dimensional conduction in the pillar. The heating power supplied to the microfluidic flow boiling structure is derived as well from the vertical temperature gradient.



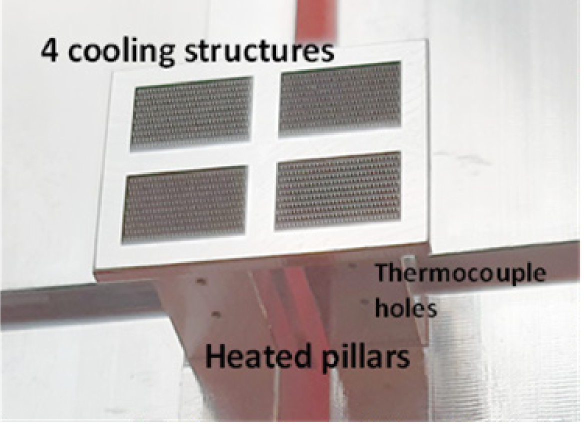
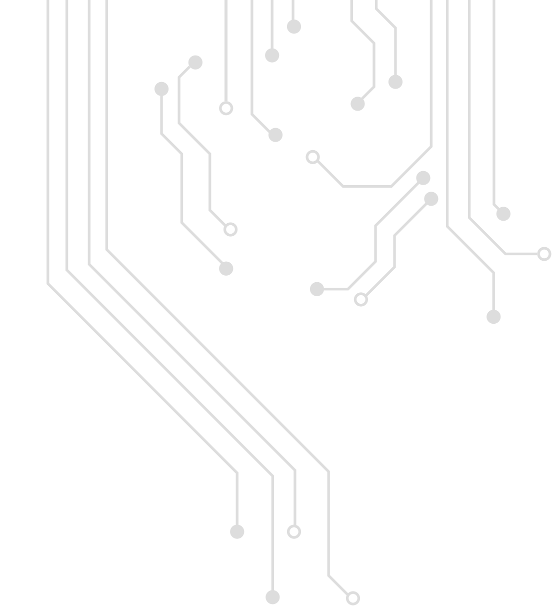


Fig. 4 Left: top side with half-bridge chips, and bottom side with TNO microfluidic flow boiling cooler structure. Right: Aluminum mockup setup with the pillars to mimic the chip heat load and the thermocouple holes to estimate the heat flux and wall temperature



The temperature at the virtual chip interface and the microfluidic flow boiling heat transfer coefficient are determined for various chip powers. Fig. 5 (left), shows the chip interface temperature. Even for the highest power it remains slightly below 90°C. Using a typical internal chip resistance of about 0.8 K/W the junction temperature remains below 120°C at a chip dissipation of 40 W. Furthermore, the temperature is little dependent on the flow rate for one chip.

The heat transfer coefficient graph (right graph of Fig. 5) shows the model results with inclusion of the surface tension. A nice correspondence with the experiments is found. Both the near independence on the flow rate as well as the slight increase on increasing heat flux is captured by the model.

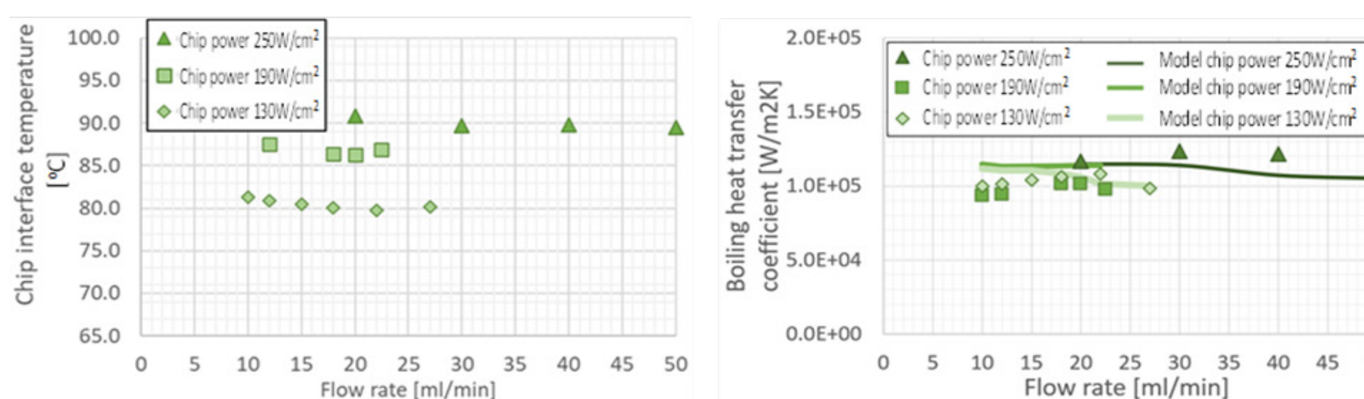


Fig. 5 Microfluidic flow boiling results: experiments (markers) and model (lines). Left: (virtual) chip interface temperature for three individual chip powers. Right: estimated microfluidic flow boiling heat transfer coefficient

TANGIBLE RESULTS

The cooling performance of the microfluidic cooler containing the TNO microfluidic flow boiling method is measured by quantifying the chip interface temperature and the microfluidic flow boiling heat transfer coefficient. For the maximum investigated chip heat flux of 250 W/cm² the chip interface temperature remained below 90°C , which implies a junction temperature below 120°C. The low pressure drops (less than 100 mbar) over the microfluidic cooler are invoked by the low required liquid flow rates (far below 1 l/min for 1 kW heat removal). This leads to low pumping powers for the overall system.

The improved microfluidic flow boiling model captures the measured trends such as the increase of heat transfer coefficient on increasing the input heat flux and its relative independence on mass flow rate. The improved microfluidic modelling can be applied to design innovative cooler geometries for future cooling solutions, such as battery cooling and the integrated cooling of the housing of the electro-engine itself.

COMPACT AND HIGHLY EFFICIENT ELECTRICAL DRIVETRAINS

INTRODUCTION

In the pursuit of greater energy efficiency, optimizing electric powertrains has become a central focus, as their design directly affects the performance, efficiency, and competitiveness of electric vehicles (EVs). A key aspect of this optimization is the integration of critical components, such as traction inverters, DC/DC converters, and onboard chargers (OBCs), which play a significant role in energy management and overall vehicle reliability. One of the most promising advancements in electric powertrain design is the development of highly integrated solutions. By optimizing system-level efficiency and reducing the volume of components, manufacturers can enhance vehicle performance while minimizing environmental impact. This integrated approach not only improves the powertrain's performance but also simplifies the vehicle architecture, creating a more user-friendly and efficient product. In parallel, the adoption of modular architectures further contributes to scalability and system reliability. This approach enables manufacturers to accommodate diverse vehicle platforms while ensuring that future technological advancements can be seamlessly integrated.

PROGRESS BEYOND STATE OF THE ART

The HiEFFICIENT project is making significant progress beyond the state of the art in electric vehicle (EV) powertrain technology. A key area of innovation is the integration of bidirectional On-Board Chargers (OBCs) and DC/DC converters. By leveraging advanced semiconductor technologies like Silicon Carbide (SiC) and Gallium Nitride (GaN), HiEFFICIENT achieves higher efficiency and power densities (3.6 kW to 22 kW) than current market standards, while incorporating Vehicle-to-Grid (V2G) functionality to enhance grid compatibility. A major leap forward in the project is its use of in-wheel motor (IWM) technology. While IWMs are recognized for their potential in

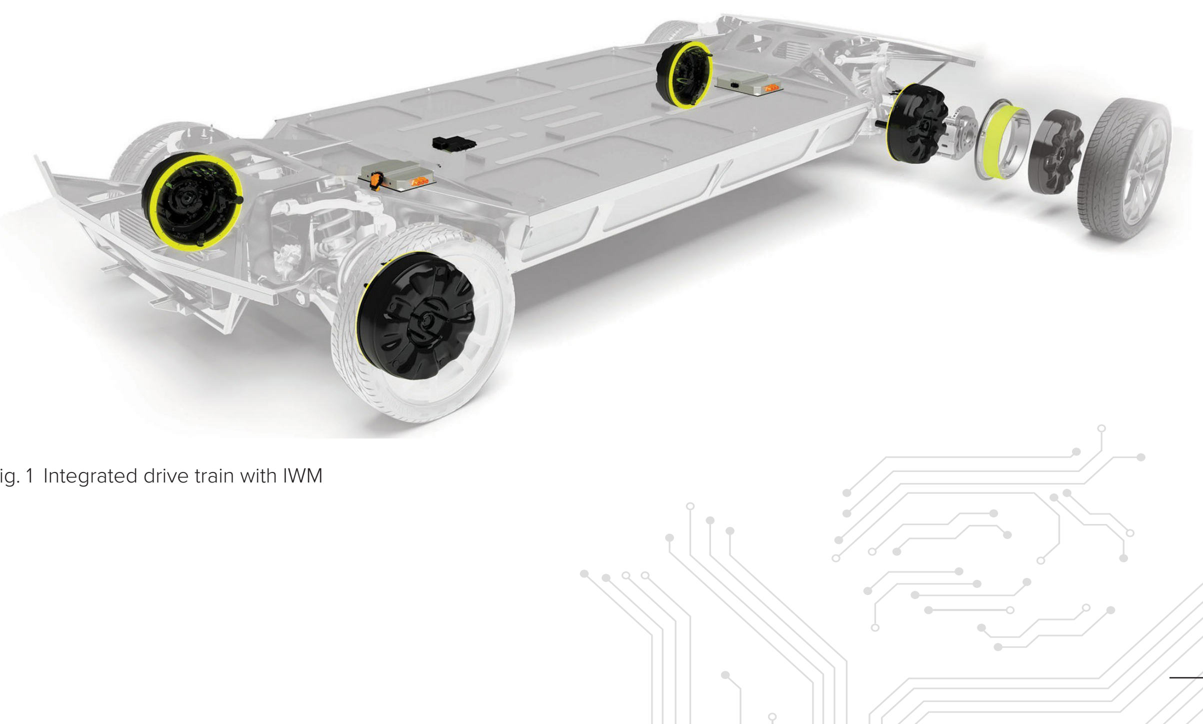


Fig. 1 Integrated drive train with IWM

EVs, HiEFFICIENT advances this by integrating highly responsive torque vectoring and eliminating mechanical links such as driveshafts. This approach improves vehicle agility, handling, and drivability by enabling instantaneous control of torque distribution, especially during cornering, acceleration, and braking. The project's use of Elaphe IWMs further refines vehicle dynamics, marking a notable advancement in torque control systems. Another key innovation is the dual inverter platform, which supports IWM systems by integrating two independent three-phase inverters in a single housing. This not only improves safety and reduces latency in torque vectoring but also lowers system complexity and costs, representing a practical solution for scalable EV architectures. The dual inverter setup ensures redundancy in case of motor failure, enabling more precise control and system resilience compared to conventional setups. HiEFFICIENT also pushes the boundaries in control response speed and bandwidth, addressing a critical limitation in traditional EV powertrains. By using direct-drive motors, the project achieves response rates far faster than the conventional 10 Hz limit, crucial for advanced driver-assistance systems (ADAS) and future autonomous vehicles. In summary, HiEFFICIENT advances the state of the art by improving powertrain integration, control precision, and efficiency. Its innovative use of IWMs, dual inverters, and advanced semiconductors sets new benchmarks for the next generation of high-performance, agile, and energy-efficient electric vehicles.

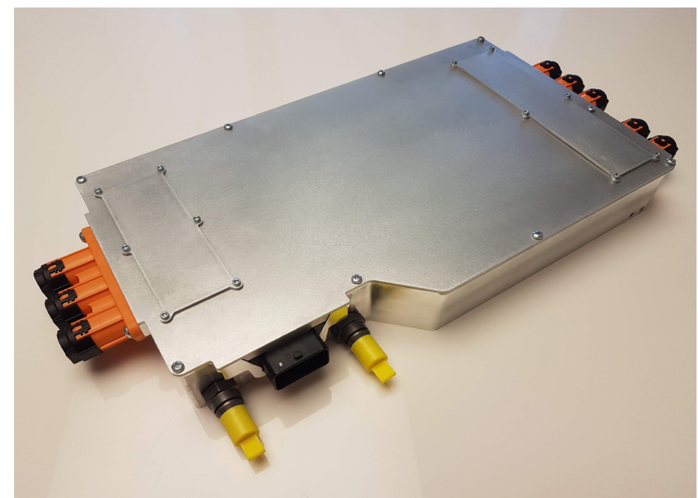


Fig. 2 Multidrive inverter

TANGIBLE RESULTS

Within the HiEFFICIENT project a most compact powertrain has been demonstrated. The smart multidrive unit developed in UC2a can drive up to two motors for a total output power in the range of 500 kW occupying a volume of just 7.5 liters, including power connections and EMC filters. The unit provides a power density close to 70 kW/l (starting from 50 kW/l developed in HiPERFORM, but having no EMC filter at this point in time!) which is an outstanding value in the 400 V battery voltage range.

As another example, the integrated OBC+DC/DC converter developed in UC5c advances component integration by incorporating a bidirectional 3 kW DC/DC converter into a 22 kW OBC architecture. The resulting unit occupies approximately 13.7 liters, representing a volume reduction of over 15% compared to conventional standalone components. The efficiency between AC and HV DC reaches around 94-95%, while for the low-voltage DC section, we anticipate an efficiency above 92%.

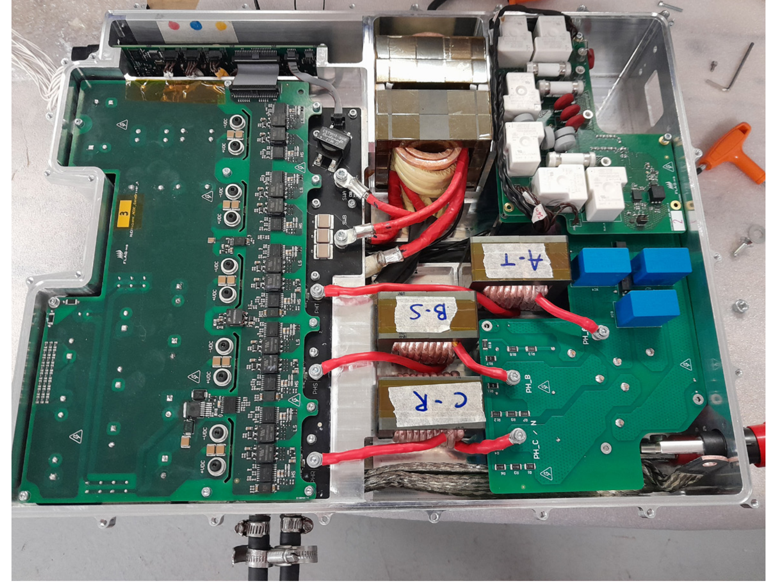
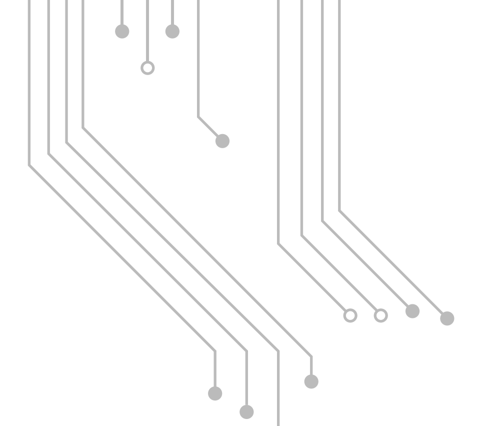


Fig. 3 Integrated OBC + DC/DC converter



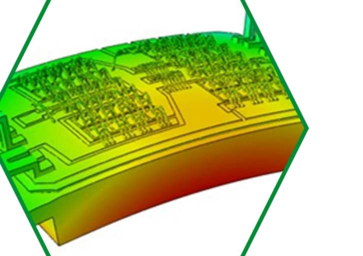
HIGHLIGHTS KEY RESULTS

KEY RESULT 1 - FIRST GAN SIP AND SOC DEVICES OUT OF EUROPE

- 100 V SoC on GaN-on-SOI substrates
- 650 V SoC on GaN-on-poly-AlN substrates
- 100 V SiP half-bridge

KEY RESULT 2 - INTEGRATION METHODOLOGIES AND CONCEPTS FOR HIGH POWER AUTOMOTIVE POWER ELECTRONICS

- 1200 V SiC half-bridge embedded in PCB
- 650 V GaN SoC on polyAlN embedded in PCB
- Sinterlamination with Cu-paste
- Highly reliable packaging concepts exceeding 500,000 power cycles under harsh conditions



KEY RESULT 3 - MAKE RELIABILITY AND PHM FUNCTIONS VISIBLE AT THE TOP SYSTEM LEVEL AND TO THE END USER

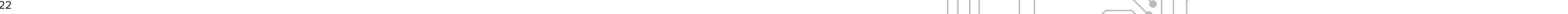
- Hybrid DD-PoF model
- Mission-profile-oriented reliability assessment tool for optimized design for reliability
- Active thermal control concepts to minimize thermal cycling
- Non-invasive junction temperature measurement with high bandwidth
- Mission profile oriented lifetime test system

KEY RESULT 4 - ADVANCED COOLING CONCEPTS FOR HIGHLY INTEGRATED POWER ELECTRONICS

- Microfluidic flow boiling capable of 250 W/cm^2 heat flux

KEY RESULT 5 - COMPACT AND HIGHLY EFFICIENT ELECTRICAL DRIVETRAINS

- Multidrive inverter with 70 kW/l power density
- Integrated OBC+DC/DC converter with 1.6 kW/l power density
- OBC with 7 kw/l power density



UC1

ELECTRIFICATION TEST SYSTEMS USING MODULAR CONCEPTS AND EMBEDDED POWER ELECTRONICS

Use case 1 focused on the development of test systems for validating the key electric and electronic components in electrified vehicles (EVs). Thereby three different focus topics have been followed, covering flexible converters with reduced size and new power levels, Prognostic Health Management (PHM) for power electronics in electrification testbeds and testing equipment for automotive power electronics lifetime testing.

In order to facilitate the shift towards electric mobility on a large scale, it is necessary to build massive test infrastructure for R&D, validation and quality assurance during production of all in-vehicle components as well as charging equipment. To keep the environmental impact low, this infrastructure must be built with a small ecological footprint and operated with low energy consumption. Designing compact, efficient and high dynamic power converters for test systems is a key element for achieving this goal.

When looking at the development of electrified vehicles in more detail, there is a need for cost efficient but high-fidelity testing solutions that replicates later customer usage as close as possible. Additionally, as the market evolves, testing requirements are getting broader and more complex. Hence, there is a strong need for flexible testing equipment, which can fulfil the needs of both component and vehicle manufactures. Particularly, Power-Hardware-in-the-Loop systems (P-HIL) are highly valued for the automated performance and lifetime testing of electric mobility components, like batteries, or any types of converters. Within the P-HIL concept, the environment of the devices under test is emulated by power electronic converters. These converters have high signal quality requirements, which can only be achieved by using high frequency switching, digitally controlled amplifiers. The high switching frequency combined with optimized topologies and filters yields smooth signals up to a high bandwidth, prerequisite for accurately emulating component details, e.g., stray inductances of electric motors. Having said this, electrification test systems are therefore a challenging but ideal application field for wide-bandgap (WBG) semiconductors. Indeed, WBG devices are a necessity to achieve very high-fidelity emulating testing systems.

Along with the requirements for exceptional performance comes the need for a reliable and predictable operation of these solutions to minimize operational costs. Consequently, advanced power electronics control strategies and operation data analytics are important for a continuous and optimized operation.

To deliver the next generation of such test systems, following topics were in focus:

UC1a Flexible converters with reduced size and new power levels

- *1200 V SiC based power converter*
- *650 V GaN based digital amplifier*
- *High performance control platform*

UC1b Prognostic Health Management for power electronics in electrification testbeds

- *2 different approaches for Condition Monitoring and optimized operation*
- *Data analytics of operational data for failure prognosis*

UC1c Testing equipment for automotive power electronics lifetime testing

UC1A

FLEXIBLE CONVERTERS WITH REDUCED SIZE AND NEW POWER LEVELS

Until today, so-called power stacks are used to build power converters for such applications. These power stacks are an assembly of discrete components: power semiconductor packages mounted on cooling plates, DC-link & snubber capacitors, high-current busbars, gate drive circuits and mounting frames.

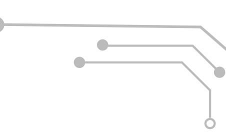
Typically, one stack is used for one application, which is designed for a given voltage and power level with a fixed number of phase legs and a target switching frequency. Any change of these parameters requires a time-consuming re-design and re-qualification of the entire stack, which limits the freedom in designing the test systems. One of the major challenges in power stack design is the ambivalence of the interface between power semiconductors and the cooling plate: it shall provide as low thermal resistance as possible on one hand, but it must also provide electrical insulation for reliable and safe operation. Most commonly, two different approaches are used to bridge this gap. One is the design of converters with discrete power transistors in various forms of packages that provide relatively low thermal resistance but no electrical insulation. It is the converter designer's responsibility to ensure electrical insulation by using appropriate interface material between power transistor package and the heatsink or cooling plate. The choice of interface material defines the trade-off between cooling and insulation. Although it provides design freedom, it is also prone to sub-optimal design and design errors. Individual designs often lack the certainty of production quality and long field experience.

The other approach is to use ready-made power modules containing multiple transistors forming one or more half-bridges. These power modules already combine electrical insulation with optimized thermal conductivity. However, the composition of such modules is complex with several layers of materials with very different physical properties, bonded high-current conductors, substrate and filling materials. Such modules are difficult to manufacture with many production steps and thus expensive. The selection of predesigned modules limits the design freedom for new power converters.

Alongside the course of this project, also the state-of-the-art progressed further with new technologies appearing on the market, such as top side cooled discrete packages for low power applications or double-sided cooling modules for automotive traction converters.

Consequently, one area of development within UC1 have been power converters (DC/DC and DC/AC) and control platforms, which are, e.g., used for battery pack and module testing, battery emulation equipment and for powering e-machines. Thereby a focus was on a scalable composition of electrification testing equipment catering different applications and testing requirements from a minimum number of base modules and consequently

This UC was conducted in a collaboration of six partners:
AVL, AT&S, FHG, FHJ, IFAG, TNO



The contributions of each partner are described as follows:

AVL (UC LEAD): system specifications and design (PE, PHM), thermal simulations, micro-fluidic cooling circuit, control and P-HIL platforms

AT&S: embedded 1200 V SiC half-bridge power modules

FHG: support in chip metallization for chips embedding

FHJ: design and development of 1200 V SiC and 650 V GaN power converters

IFAG: providing 1200 V SiC dies

TNO: micro fluidic two-phase cooler for 650 V GaN power converter

following aspects were of main interest:

- Flexibility via modularity of testing equipment, to support different voltage and current ranges
- Creating compact, reduced size systems via high integration, e.g., embedding of power electronics with optimized cooling concepts.

This concept of modularity is illustrated in Fig. 1. By designing different filters, the converters can be adapted to different testing needs. By parallel connection, the power can be scaled. And by changing the application control firmware, the test system can be switched between testing and emulating various types of units under test (UUTs), e.g. batteries. To achieve the set goals three main topics have been addressed in this sub use case:

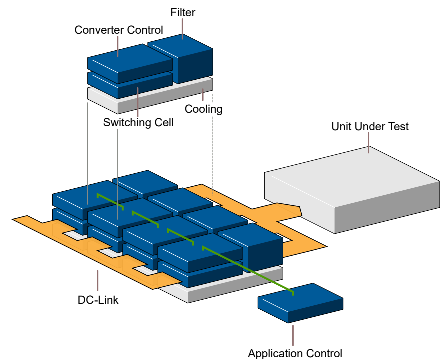


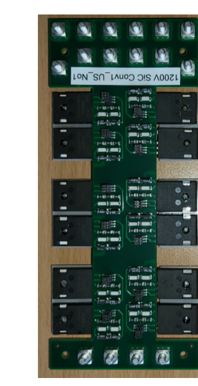
Fig. 1 Modular composition of power converters for test systems

- 1200 V SiC based switching cell for different power converter applications, with a focus on PCB-embedding of power semiconductors for application voltages up to 1000 V DC
- 650 V GaN based digital amplifier making use of an advanced cooling system
- High performance control platform to combine numerous power stacks to achieve different power and voltage levels as well as supporting latest Power-Hardware-in-the-Loop (P-HIL) application requirements

RESULTS

The initial subject covered in UC1a was the examination of the benefits of integrating chips directly into the PCB as opposed to traditional SMD-based approaches. The goal was to demonstrate advantages in power density and reliability. Therefore, project partners focused on two different implementations of a SiC switching cell for AVL's electrification testing solutions, guiding future application specs in a most compact format. FHJ thereby developed the reference design, using a discrete approach with 1200 V SiC-Mosfets in TO-247 casing. In parallel, AT&S created a half-bridge switching cell module, whereby 1200 V SiC Mosfets were embedded in the PCB. Each switching cell variant contains six half-bridges, applicable for, e.g., grid-tie-inverters, resonant-converters with galvanic isolation, DC/DC step-down converters or DC/AC inverters, but having the same form factor and hence being easily replaceable for comparison (Fig. 2). These two switching cell variants were chosen to study differences in loop inductance, thermal behaviour, and mechanical design. The developed prototypes achieved a 47% volume reduction in relation to today's baseline solution, achieving a power density of 6.4 kW/l. A certain aspect to achieve compact solutions and a reliable operation, is the thermal management. Therefore, a very efficient operation at high switching frequencies, i.e., 140 kHz, is key. Due to the potentials of power electronics embedding, the loop inductance compared to the reference design could be halved. Furthermore, detailed investigations have been conducted to achieve the best possible thermal conductivity for most efficient cooling.

A matching grid-tie inverter filter was designed to build the first application converter with this SiC stack, which is shown in Fig. 3. Due to the embedding of dies in the PCB, the reliability of such power modules can be improved compared to other packages using wire bonds. Therefore, power cycling tests of the TO-247



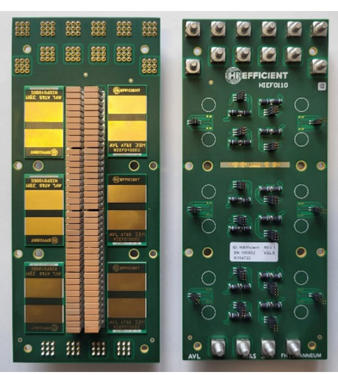


Fig. 2 Reference design and embedded and assembled SiC stack

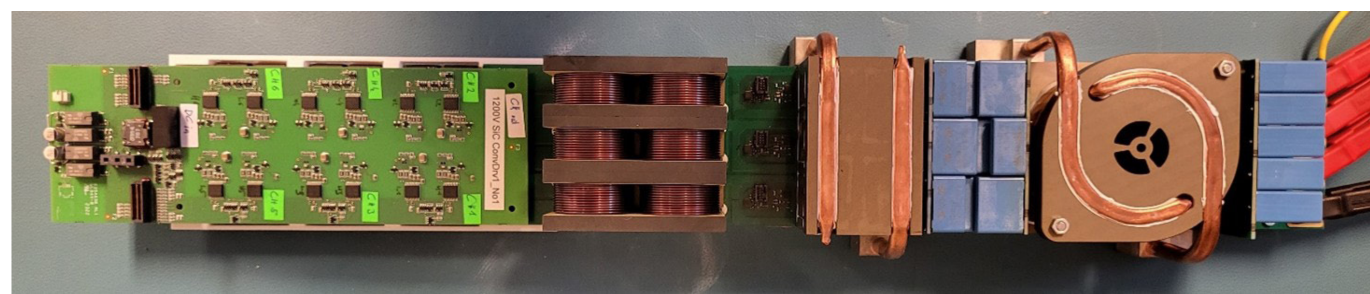


Fig. 3 125 kW SiC grid-tie inverter

and embedded SiC were carried out to benchmark the new modules. An impressive increase in lifetime was observed for the embedded devices compared to the discrete ones under comparable load conditions (junction temperature amplitude of 140 K). The TO-247 reference samples lasted up to 9000 cycles. Device failure was indicated by an increase in voltage drop. A following physical failure analysis confirmed this, showing crack growth along the bond wire foot. The embedded half-bridge modules lasted over 500,000 cycles to the end of the project. No electrical degradation has been observed to date and tests are still continued.

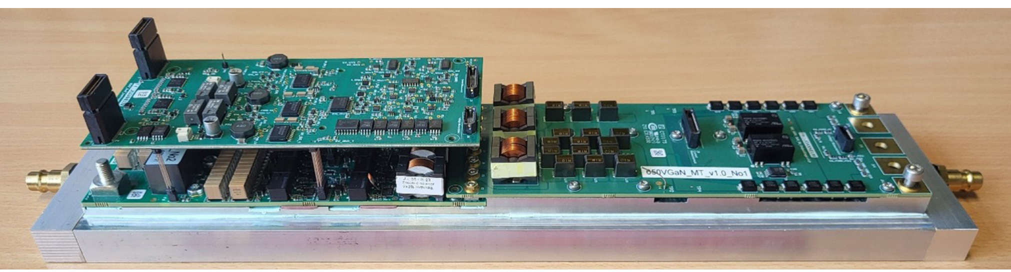


Fig. 4 90 kW GaN digital amplifier design for 2.5 MHz interleaved switching frequency

Secondly, a 650 V GaN based digital amplifier has been developd. Again, a part of the design was implemented with two different technologies with the goal to make a comparison in the same application use case. The very small GaN transistors pose a problem with very high heat dissipation per unit area. Hence, two different cooling concepts have been tailored to the GaN digital amplifier stack: a classical approach with a contour-milled aluminum cold plate and a single channel for liquid cooling (Fig. 4) and a novel micro-fluidic cooling approach with a micro-structured aluminum nitride electric insulator that facilitates superior heat transfer with a smooth, continuous boiling process (Fig. 5). Please also refer to the key result section on advanced cooling concepts with more details.

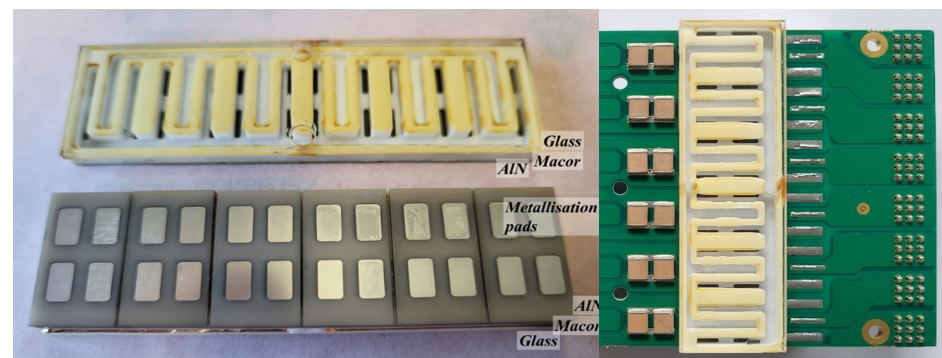


Fig. 5 Micro-fluidic cooler assembly (left) attached to the bottom side of the GaN amplifier (right)

Prototypes of the basic switching cell could be tested successfully up to 30 A per pair of coupled half-bridges at a DC-link input voltage of 400 V. The full amplifier contains 6 such half-bridge pairs, resulting in a total output current of 180 A DC. Simulation studies indicate that this amplifier will be able to achieve a voltage slew rate of 300 V in less than 10 µs at the filtered output with a steady state ripple lower than 0.15 Vpp. This allows the emulation of DC and AC grids with a high fidelity and a bandwidth of 150 kHz as an example. The goal is to replicate not only the harmonics of the grid frequency or the residual ripple of a DC bus but also parasitic impedances of cable connections. Not only for this use case, but for power electronics in general, 3D studies of liquid cooling are essential because local flow characteristics on the coolant side have a significant impact on cooling effectiveness and hot spots.

Beside classical thermal response studies, such as conjugate heat transfer in structures and single-phase cooling approach in fluid domains, the focus of this work was more on the proper simulation of the cooling design for a liquid cooling system to picture the cooling performance in a more accurate way. A 3D-CFD simulation of a multiphase phase evaporation cooling is the proper approach to investigate such kind of problems. The simulation domain is displayed in Fig. 6 (top) showing one segment with four GaN chips on top of the multi-layer solid structure. In this illustrated example, the four chips provide a heat input of 4 x 20 W into the segment. A fluid mixture is entering the domain with a temperature of 35 °C. The applied RPI (Rensselaer Polytechnic Institute) wall boiling model is an advanced approach to deal with the nucleate boiling regime. The basic model assumes that the vapor phase is always at saturation conditions and only evaporation is modelled due to heated walls (defined as temperature or heat flux boundary conditions, or multi-material interfaces). A major target in this simulation is the average temperature at the interface between the chips and the interposer material which is kept at approx. 83 °C which is well within specified limits.

Due to the wide range of different setups that can be generated with different combinations of approaches, sub-models, and boundary conditions specification, the improvement of the model stability is able to consider many different aspects.

As a qualitative measure the distribution of the built-up of the vapor volume fraction of the coolant is also checked (Fig. 6 (bottom)). Together with other quantities, such as flow field parameters, it provides ideas to improve the flow path and thus also the heat transfer. The final design of the micro-fluidic cooling assembly could be tested in a dedicated test setup. With a power dissipation of 20 W per chip (total: 48 chips per amplifier) and an elevated inlet temperature of 60°C, a surprisingly low flow rate of less than 5 ml/min per chip is required to keep the junction temperature at a maximum of 110°C. This makes it possible to use a simple condenser to dissipate the waste heat to the ambient air without an additional chiller.

Alongside the development of modular power building blocks, a cutting-edge control platform has been devised, enabling the flexible combination of multiple power stacks either in parallel or series to meet specific requirements for voltage and current in various applications. The research also prioritised the advancement of Power-Hardware-in-the-Loop (P-HIL) solutions, which are crucial for the automated testing of electric mobility components. Central to this P-HIL system is a versatile power stack paired with a control unit capable of functioning across different applications by adapting the control software and related components like filters and inductors. The power stacks developed in UC1a will be integrated into this setup, catering to diverse testing scenarios.

IMPACT OF UC1A

The technology developed within this use case is a great step forward in manufacturability of high power density converters. It allows more parts to be integrated into PCBs, thus reducing the need for interconnections with cables and busbars. Although the complexity of the PCBs themselves certainly rises, the number of assembly steps for the converters can be reduced and the high degree of automation provides economies of scale to reduce cost, optimize material usage and greatly improve quality.

The resulting compact converter modules can be arranged in different applications. They can be scaled in power, current, and voltage. Combined with greatly increased robustness and lifetime, the resulting test systems can be used for many years, even with high utilization. The long operation life also reduces the ecological impact of manufacturing.

The tight integration reduces parasitic loop inductance such that the full advantage of the SiC semiconductors can be utilized for high dynamic output control and higher efficiency. The consequent reduction of filter size also contributes to the reduction of raw material usage and converter size and thus the environmental impact.

Furthermore, UC1a was setup with dedicated interfaces between the individual functional layers, such that technologies can be exchanged within the layers and meaningful benchmarks can be executed in comparable settings. This allows for careful selection of technologies and variants on the way towards product development. It is possible to evaluate power traditional semiconductor packaging compared to PCB embedding, different cooling concepts, gate drive, and control circuitry – all independently of each other.

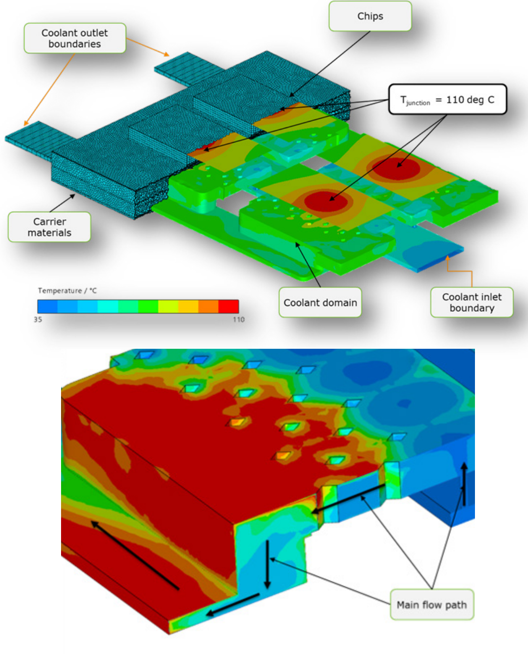


Fig. 6 Simulation domain (top) and vapour formation along the flow path (bottom)

The applied simulation approach for the evaporation cooling provides the proper tools to start investigations in an early stage of the design because local flow characteristics on the coolant side have a significant impact on cooling and its performance. And problems which are detected early in advance can avoid expensive cycles of iteration during prototyping and manufacturing phase.

Furthermore, the application of these physical models includes most of the thermal management systems (e.g., general cooling phenomena in power electronics, water cooling jacket, battery cooling) in which evaporation phenomena are used to absorb heat and carry it out of the system.

UC1a Achievements

- 47% volume reduction
- GaN amplifier with 625 kHz switching frequency and 2.5 MHz ripple frequency
- 250 W/cm² heat transfer with reduced cooling system size: 90% reduction in size and flow rate

- 50 times longer lifetime of embedded 1200 V SiC half-bridge modules compared to conventional TO-247 packages

- Single control platform for multiple converter control

UC1B

PROGNOSTIC HEALTH MANAGEMENT FOR POWER ELECTRONICS IN ELECTRIFICATION TESTBEDS

The UC1b demonstrators assessed the feasibility of condition monitoring and Prognostic Health Management (PHM) to improve power electronics in electrification test fields through three solutions. The first approach used gate driver manipulation to maintain constant losses, and the second employed non-invasive temperature measurements to adapt system performance. The final data-driven method, developed with UC2a, analysed logged parameters to determine system health. All methods were tested on scaled-down versions of the potential target platform using identical components for straightforward proof of concept.

RESULTS

Gate driver manipulation

As a part of the project, a detailed power loss model has been developed to estimate conduction and switching losses of a multi-chip SiC power module, using manufacturer data and electrical parameters. In addition to that, a compact thermal model of the power module was also created.

Based on the electrothermal model, an observer-based real-time electrothermal condition monitoring system was designed for inverter systems. It uses the temperature sensor integrated into the power module to estimate the junction temperature. Moreover, an adaptive gate driver system was developed to manipulate gate voltage and control the junction temperature, effectively reducing thermal cycling. Laboratory tests showed that the Active Thermal Control (ATC) system reduced thermal cycles, potentially enhancing the lifespan of the power module.

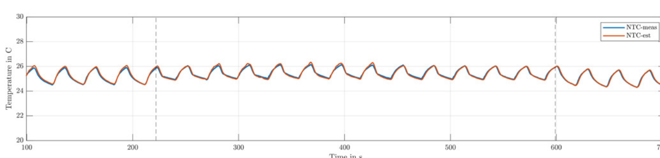


Fig. 1 Operation of the observer-based condition monitoring system

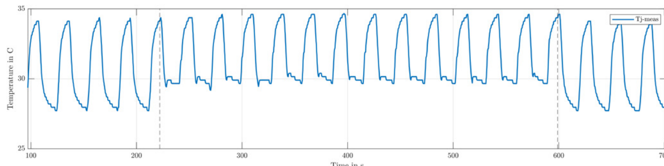


Fig. 2 Operation of the active thermal control system

This UC was conducted in a collaboration of four partners:
AVL, RWTH, SAL, VIF

The contributions of each partner are described as follows:

AVL (UC LEAD): system requirements and provision of test vehicle

RWTH: 3D and compact thermal modelling of the multi-chip power module; real-time condition monitoring and active thermal control systems

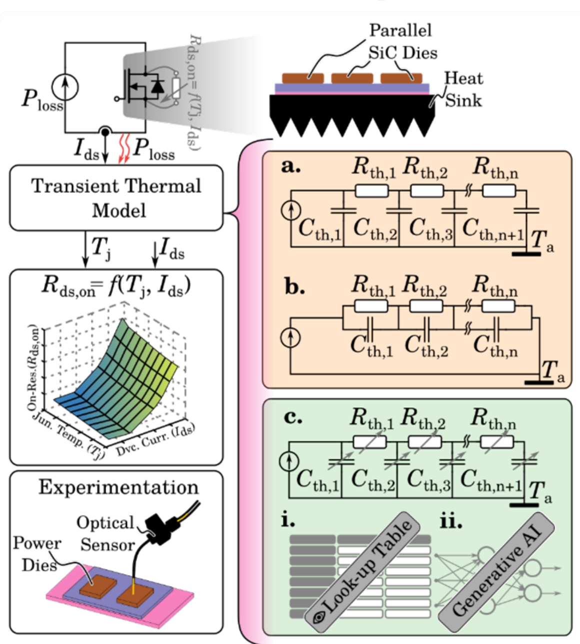
SAL: real time condition monitoring based on virtual junction temperature estimation

VIF: data-driven modelling on reliability and PHM

Non-invasive Thermal Control

UC1b further includes the development and integration of a non-invasive thermal control system aimed at enhancing the lifespan of SiC MOSFETs. A key contribution is the development of a transient thermal model for real-time estimation of the junction temperatures (T_j) within the power module. This model is trained using both synthetic and experimental thermal data to optimize thermal management. Integrated into the UC1b's inverter topology, the system uses real-time temperature data to dynamically adjust switching patterns, minimizing thermal load and optimizing the performance of the power electronics.

The non-invasive thermal control system involves transient thermal characterization of SiC MOSFETs in the UC1b demonstrator, validated through both simulation and experimental frameworks using the CAS480M12HM3 SiC power module as shown in Fig. 3. Simulations are conducted in MATLAB/Simulink and PLECS environments and compared with experimental data from Opsens GaAs fiber-optic sensors. The models include a generative adversarial network-based temperature-dependent thermal (GAN-TDT) framework for measuring temperatures across multiple dies. The GAN-TDT model is trained by optimizing the generator (G) and discriminator (D) networks over 1000 epochs using the Adam optimizer. In the closed-loop simulation, the trapezoidal rule solver (ode23t) estimates T_j iteratively, using power loss calculations to refine thermal parameters. Experimental validation, performed using fiber-optic sensors mounted on the power module cooled by a Q-ATS cold plate, measured T_j at two dies to account for thermal cross-talk. Calibration against known temperatures ensured accuracy, with average estimation errors of 2.17% for the central die and 4.52% for the peripheral die, confirming the model's effectiveness. Further, the trained model's bandwidth was assessed by calculating the power spectral density, yielding an average bandwidth of 20.03 Hz, confirming its ability to capture dominant thermal response characteristics. For the UC demonstration, the model is deployed with the simulated converter topology operated with a torque profile and the average estimated temperatures for the power module operation are shown in Fig. 4.



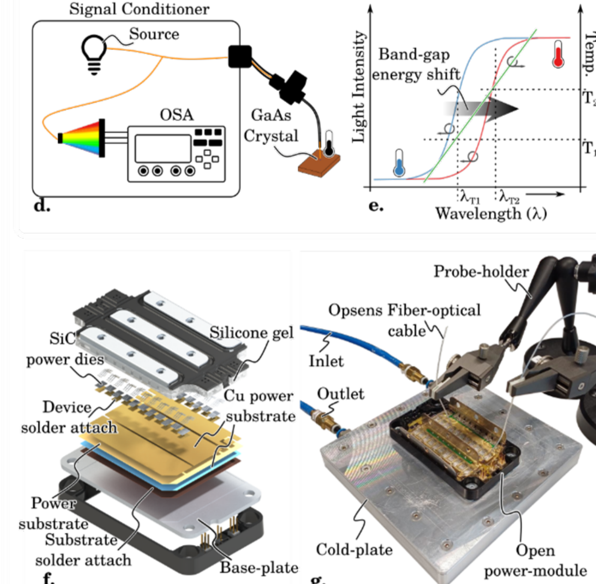


Fig. 3 Process flow for transient thermal characterization. The workflow illustrates the use of (a) Cauer, (b) Foster, and (c) temperature-dependent Cauer models with (i) look-up tables and (ii) generative AI. On-state resistance is adjusted dynamically based on estimated junction temperature(T_j) from the RC thermal network and drain current. Estimated T_j is validated using fiber-optic sensors. (d) Temperature change detected via GaAs-based fiber optic measurements using an Optical Spectrum Analyzer (OSA), and (e) temperature-wavelength relationship, where higher temperatures shift the band-gap spectral position. (f) Layer stack-up of CAS480M12HM3 power module, with seven layers modelled for transient thermal analysis. (g) Hardware setup with SiC power module, fiber-optic cables, and cold-plate, measuring T_j at two paralleled dies (periphery and center) to capture thermal cross-talk

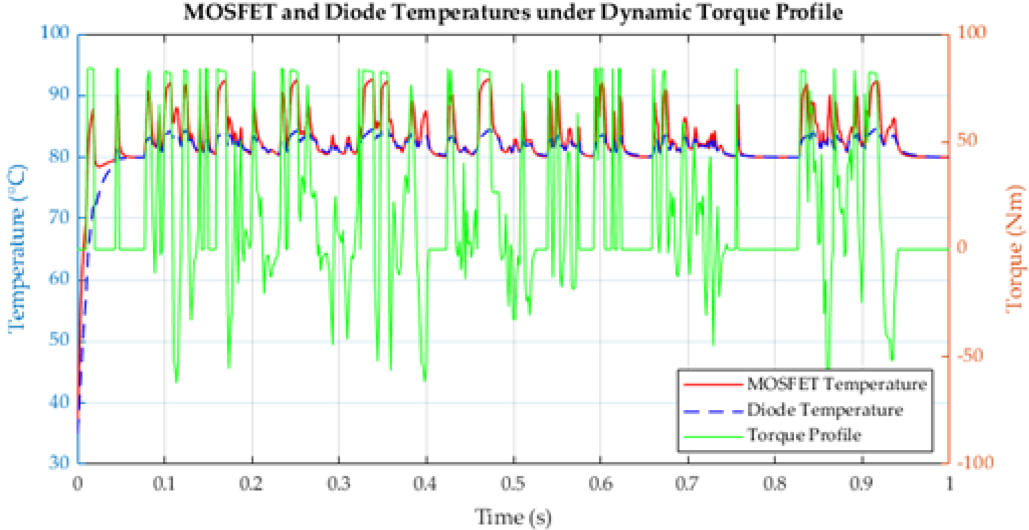


Fig. 4 Dynamic response of MOSFET and diode junction temperatures under varying torque. Solid red line denotes MOSFET temperature, blue dashed line indicates diode temperature (°C, left y-axis), and green line shows torque profile (Nm, right y-axis)

The thermal control focuses on integrating the GAN-TDT model to provide real-time temperature estimates and assess control strategies like field-oriented control (FOC) and discontinuous pulse width modulation (DPWM) to minimize converter power loss through the workflow shown in Fig. 5.

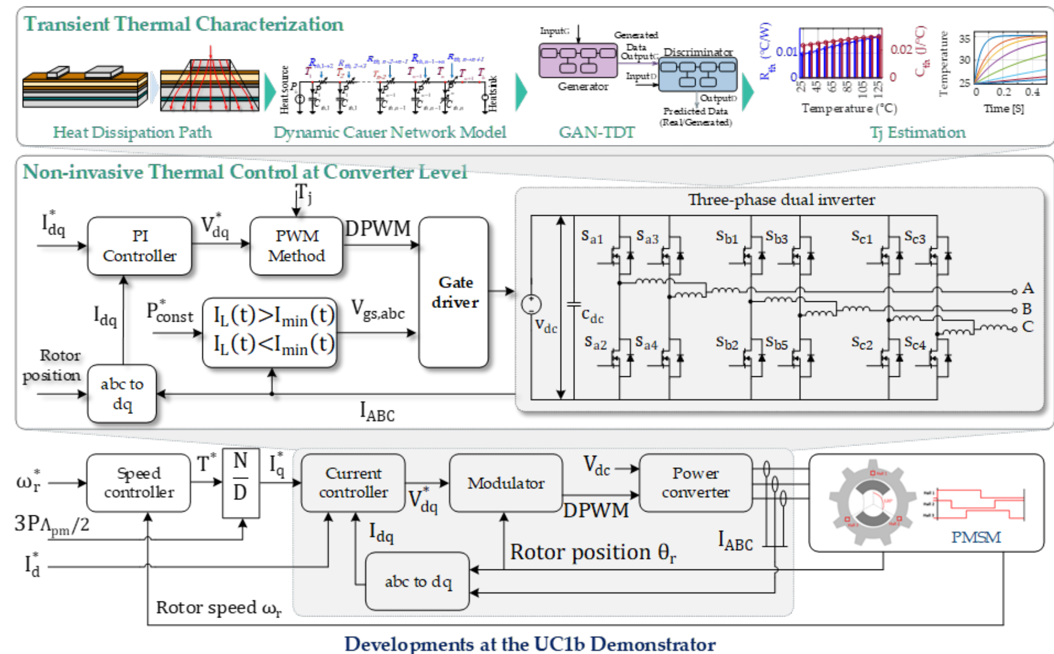


Fig. 5 Integrated Thermal Control System for SiC MOSFETs in Dual Inverter Configuration with PMSM drive. The system utilizes a GAN-TDT model for accurate junction temperature estimation and employs discontinuous pulse width modulation to optimize switching events based on thermal feedback, minimizing power loss, and reducing thermal stress

The UC1b dual inverter system was modelled in Simulink, where FOC managed torque and speed of the PMSM, while DPWM optimized switching based on estimated junction temperatures to reduce MOSFET thermal stress. The model operated under the similar torque profile as shown in Fig. 4 with a 20 kHz switching frequency. The GAN-TDT model, integrated as a custom MATLAB block, provided real-time power loss estimates to guide DPWM adjustments for effective thermal management, identifying stress points.

Simulations demonstrated balanced phase currents and stable torque control with minimal distortions. The rotor speed remained around 3000 rpm, showing the system's responsiveness to load

changes. D-axis and q-axis currents in FOC scenarios converged smoothly after minor overshoots, demonstrating effective control. Power loss comparison between FOC-SVPWM and the new thermal control system showed the latter limited power loss to under 150 W, significantly improving thermal management and overall inverter efficiency. This in turn leads to decreased thermal stress in power devices suggesting a potential lifetime extension of approximately 1.5% as shown in Fig. 6, with further experimental validation required.

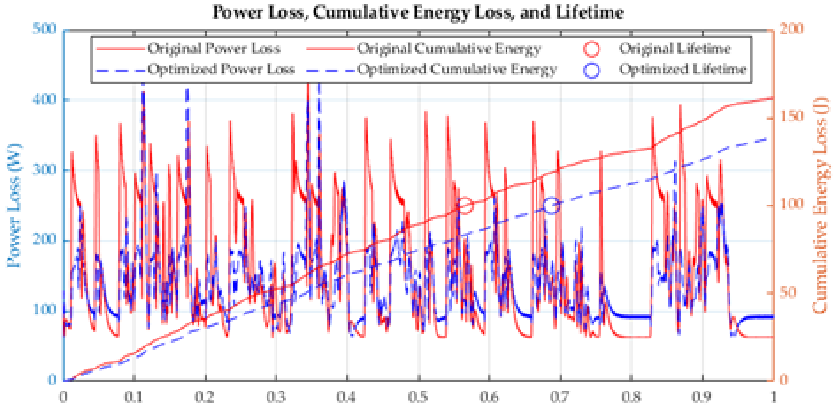


Fig. 6 Comparison of original controller and optimized thermal management systems showing power loss (W, left y-axis) and cumulative energy loss (J, right y-axis). Solid red lines indicate original power metrics, while dashed blue lines represent optimized results. Circular markers depict estimated device lifetime, highlighting a 1.5% extension achieved through reduced power loss and improved thermal efficiency

DD methodologies for health/damage prediction

The Data-Driven (DD) methodology has been developed considering the most common failure mechanisms. The following methodology is explained in detail in UC2a. As a summary, one method for estimating the State of Health (SoH) involves utilization of data-driven models, which typically necessitate extensive datasets from accelerated aging tests or condition monitoring. Considering the limited availability of such data, a MATLAB Simulink-based electro-thermal model was developed to generate data. The junction temperatures of the switches were evaluated using a Foster equivalent thermal network. This synthetic data enabled the development of Deep Neural Network (DNN) models using Convolutional Neural Networks (CNN) and Long Short-Term Memory (LSTM) NN in Python. The models can be used to estimate the SoH of SiC MOSFETs and are integrated into MATLAB Simulink for further analysis. The workflow is shown in Fig. 7.

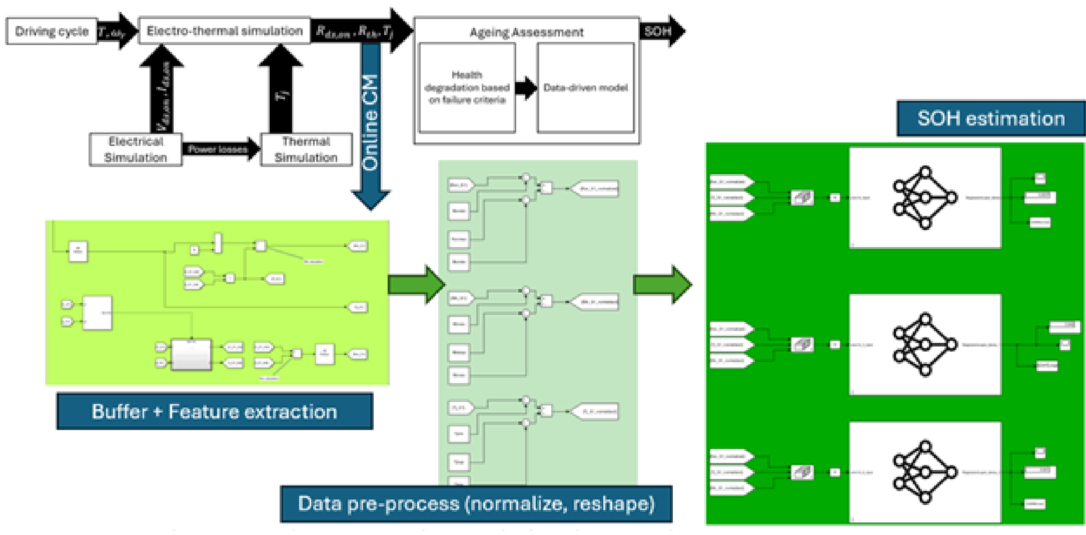


Fig. 7 Workflow of the approach including online monitoring – results from electro-thermal simulations are used for the DD model; model is altered to predict the SOH in close to real time – buffer is created to store the data - feature extraction and data preprocessing occurs and then the signals are passed on to the models for DD estimation

For Data Driven (DD) approaches, data acquisition step is naturally followed by performing feature engineering. This process is used to generate new features by forming linear combinations of existing ones, resulting in a distinct feature set, with potentially higher correlation with the label set. The selected features are $R_{ds,on}$, R_{th}, and T_j.

In supervised learning, each feature must be linked to a corresponding label, necessitating the calculation of labels based on failure criteria. These output labels, which reflect the model's predictions, are crucial for training the neural network (NN). In this study, the label represents the State of Health (SoH) of the power modules, with values ranging from 0% to 100%. A SoH of 100% indicates optimal device performance, whereas a SoH of 0% signifies that the device has reached its end of life and requires maintenance or replacement. To ensure redundancy, three methods are employed for SoH calculation, like increase of $R_{ds,on}$, R_{th} and T_j, compared to the value in the first thermal cycle. If certain thresholds are exceeded, the failure criteria are triggered for further action and respective maintenance.

Various algorithms are available within the modelling framework, which includes Convolutional Neural Network (CNN) layers and Long Short-Term Memory (LSTM) Recurrent Neural Networks (RNN) layers. This hybrid approach is particularly effective for time series data with multiple variables that benefit from convolutional operations. Enhanced feature extraction is a significant advantage, as convolutional layers identify important features before they are processed by LSTM cells. The architecture typically consists of 1D convolutional layers and max pooling layers, enabling local pattern detection and dimensionality reduction, respectively. Additionally, a rectified linear unit (ReLU) activation function is incorporated into some layers. The model employs a decayed learning rate and early stopping, with Adaptive Moment Estimation (Adam) chosen as the optimization function following a hyperparameter tuning process.

The models described above were collaboratively developed with UC2a and finally validated with UC2a data.

IMPACT OF UC1B

Within UC1b partners were able to develop innovative condition monitoring and prognostic health management concepts. The results achieved by RWTH contribute to improved thermal management and reliability of power modules, enhancing both real-time monitoring and active thermal control in high-performance applications. This proof of concept represents a significant advancement in enhancing the reliability of power electronic (PE) systems. The results demonstrate the potential for implementing online condition monitoring, utilizing established failure criteria from conducted Failure Modes, Mechanisms, and Effects Analysis (FMMEA). This approach lays the groundwork for more robust predictive maintenance strategies, directly contributing to the long-term performance and dependability of PE systems.

The integration of the non-invasive thermal control system and the GAN-TDT models by SAL in the UC1b demonstrator marks a significant advancement over conventional state-of-the-art thermal management techniques, primarily by providing more accurate real-time junction temperature estimation. Unlike traditional thermal models that often rely on simplified RC network approximations, the GAN-TDT framework utilizes machine learning to capture complex, temperature-dependent thermal behaviours across multiple dies. This enhanced accuracy allows for dynamic adjustment of switching patterns using discontinuous pulse width modulation, reducing thermal stress and power losses. Consequently, this adaptive control approach not only improves power module efficiency by maintaining lower temperatures under variable load conditions but also addresses the thermal cross-talk between dies, a common issue in conventional designs. The real-time adaptability ensures that thermal thresholds are not exceeded, reducing the need for conservative design margins and thus, enabling more efficient component usage. For end users, this leads to a longer lifespan of SiC MOSFETs, and enhanced reliability of power electronics systems.

Lastly, newly developed DD methodologies for the SoH prediction of power electronics components have been in collaboration with UC2 successfully developed, showing a good alignment between prediction and actual health status.. This will help to improve operational efficiency of power electronic systems.

UC1b Achievements

– 12% lifetime increase by using an observer-based condition monitoring and active thermal control system, using loss manipulation by actively altering the gate voltage
– 1.5% lifetime increase by using GAN-TDT model for real-time junction temperature estimation applied in active thermal control
– Non-invasive high bandwidth temperature sensing with 20 Hz

UC1C

TESTING EQUIPMENT FOR AUTOMOTIVE POWER ELECTRONICS LIFETIME TESTING

Main objective in UC1c is the development of a methodology and the according testing equipment to evaluate automotive power electronics components, e.g. inverter, with respect to their lifetime and to assess a series failure rate. Therefore, the involved partners investigated potential testing methodologies and the lifetime models for power electronic systems. Power electronics module's lifetime, expressed in number of power cycles until failure, mainly depends on the semiconductor's junction temperature swing, mean junction temperature, and the heating time. Hence, according testing methods have been investigated.

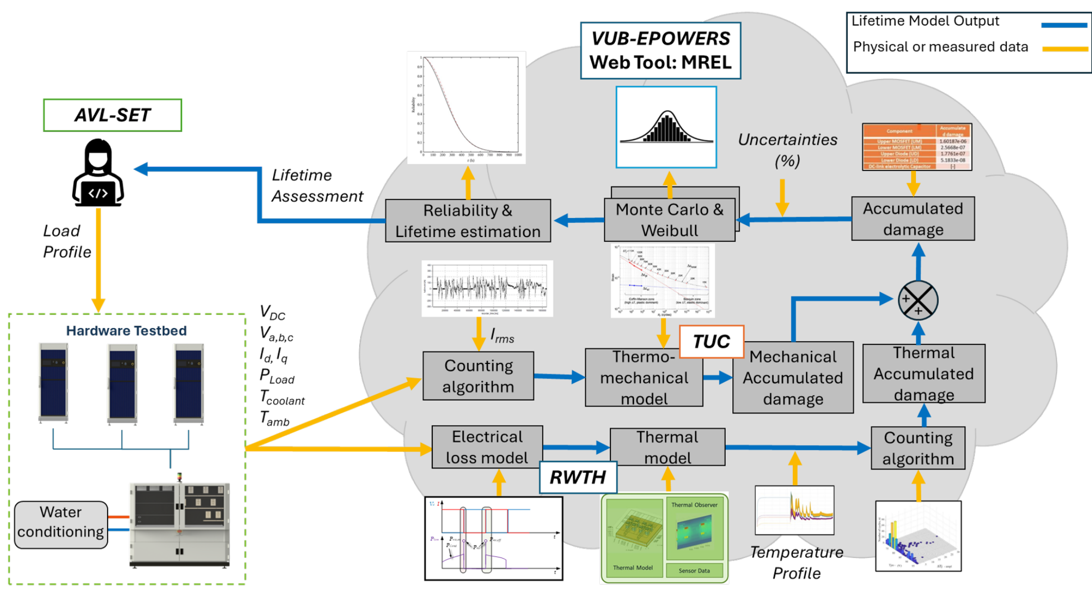


Fig. 1 UC1c system concept and partner responsibilities

This UC was conducted in a collaboration of four partners:
AVL-SET, RWTH, TUC, VUB

The contributions of each partner are described as follows:

AVL-SET (UC LEAD): developed an inverter test system

RWTH: supported with electro-thermal loss models

TUC: contributed with thermo-mechanical models

VUB: provided a web-based tool for lifetime assessment, incorporating datasets from measurement and surrogate models

RESULTS

First, an interface was developed to enable parameter recording from the Unit Under Test (UUT) via AVL PUMA 2™ Inverter, with a maximum recording frequency of 1 kHz. Parameters such as temperatures, currents, voltages, speed, torque, and coolant flow rate were collected. These parameters were measured during simulations of standard driving cycles, including WLTP, NEDC, and JC08, which were implemented using AVL VSM™. The recorded data was processed and exported in MDF4 and MAT formats through AVL Concerto, after which it was shared with other partners. This data was required for further analysis to estimate the lifecycle of power electronics components under different driving conditions. Despite the success in data collection, a limitation was noted: the system could not support recording at the desired 10 kHz frequency due to restrictions in the communication protocol. The system's 1 kHz recording frequency was aligned with the capabilities of the partner companies' models, ensuring compatibility without the need for higher frequency adjustments.

Compact electro-thermal modelling and sensor location optimization results

Similar to UC1b, the electrothermal model of the power module in this use case has been created by RWTH. The loss model of the power module in UC1b has been adjusted based on the structure of the Microsemi power module and provided test results from the manufacturer. The implemented electrothermal model has been used to simulate the losses and junction temperature of the switching devices by applying the measured data for WLTP mission profile. Fig. 3 shows the results of the performed simulation.

Furthermore, an optimization algorithm was developed to find the best locations for temperature sensors within multi-chip power modules (Fig. 4). The approach focuses on maximizing the sensor bandwidth based on the number of sensors used. Results show that placing sensors in the optimized locations enhances the accuracy of temperature measurement, providing better thermal monitoring.

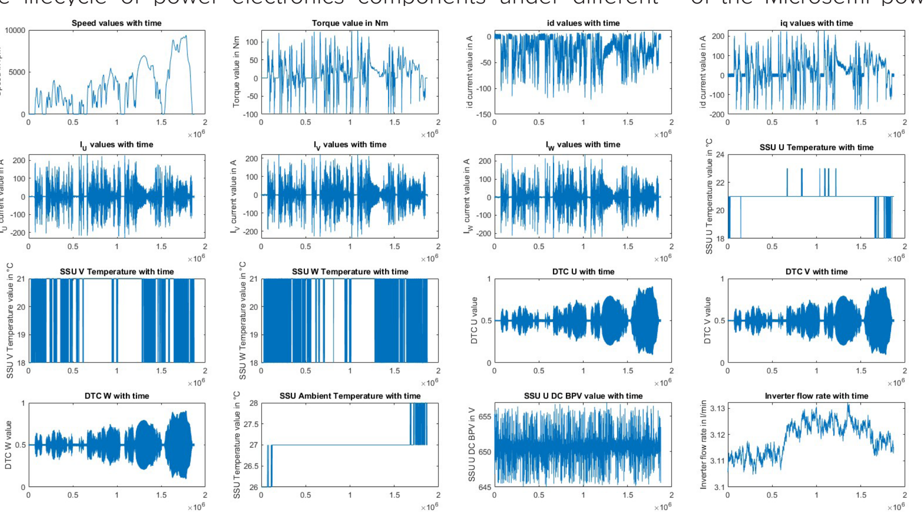


Fig. 2 UUT parameters recorded on the WLTP cycle

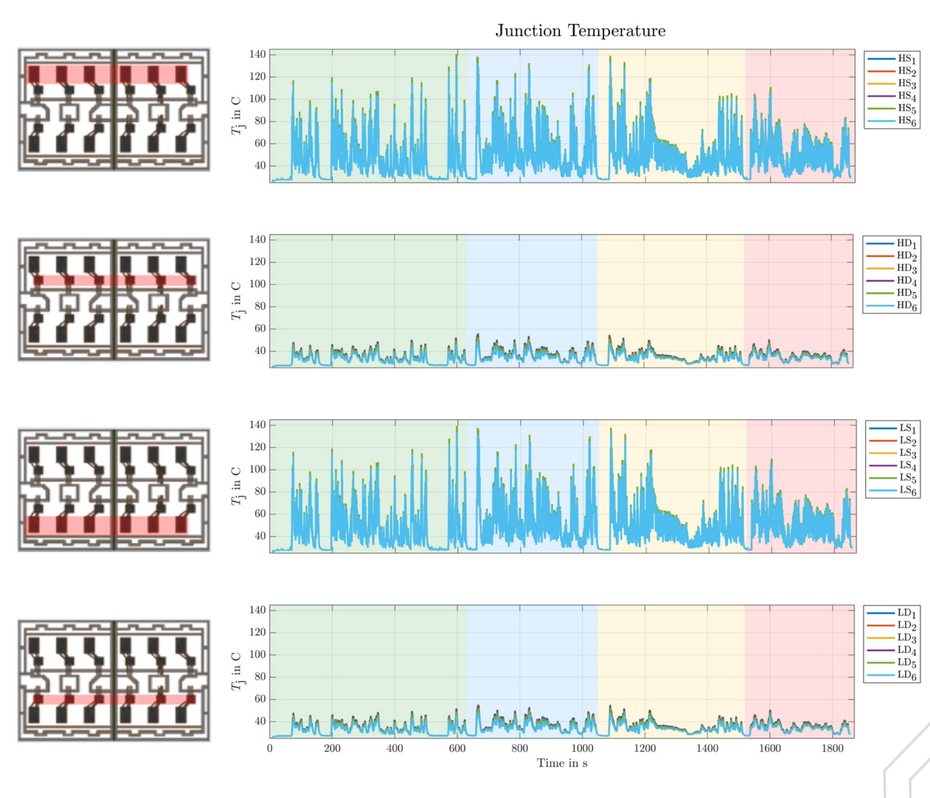


Fig. 3 Simulating junction temperature for WLTP mission profile

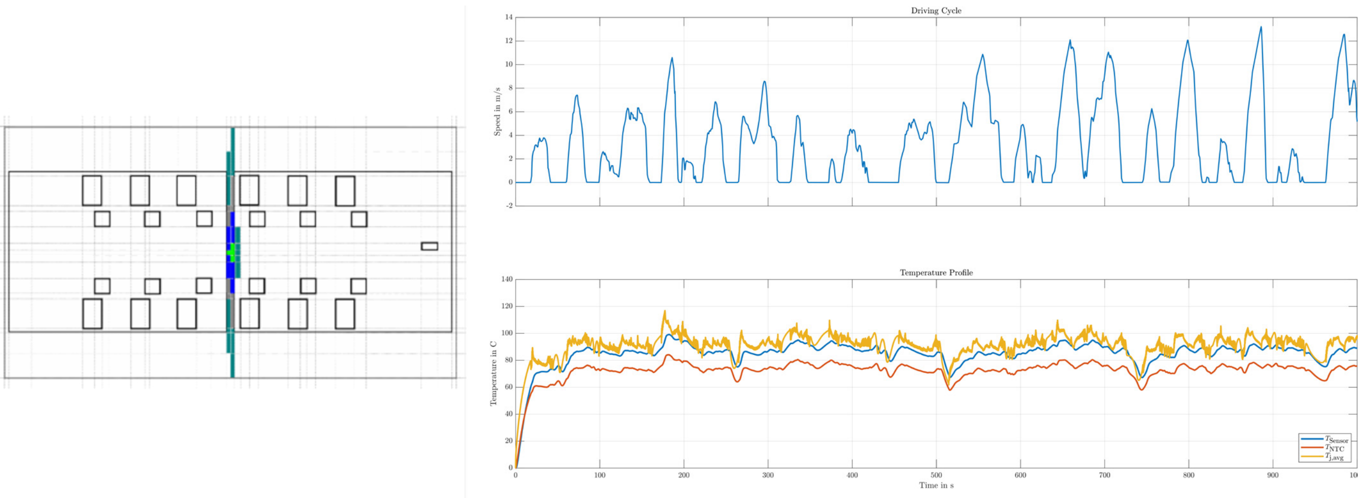


Fig. 4 Optimization of temperature sensor location inside the power module

Thermo-mechanical modelling and thermal fatigue evaluation

To assess the degradation over time, TUC created a finite element simulation model of the power module (Fig. 5). To avoid simulating a complete electrical load profile, which can be highly variable, the I(t) profile has been broken down into cycles using a rainflow counting algorithm. This extracts cycles with specific amplitudes and average current values. An electro-thermal simulation is then performed. The simulation gives the temperature field in the power module. The thermal field is then used as a load condition profile for a thermo-mechanical simulation. Based on this, the mechanical stress and strain at critical positions such as die attach and bond wire foot are analysed. The Coffin-Manson relationship is used to determine the relationship between the mechanical stresses and the number of cycles to failure. Afterward, a functional mock up (FMU) is provided to VUB for integration into the "MREL Tool: Mission-profile-oriented reliability assessment tool".

Lifetime assessment model: Combined thermal and mechanical fatigue evaluation

VUB further extended their in-house "MREL Tool: Mission-profile-oriented reliability assessment tool" to utilize it for lifetime assessment of the UC1c. VUB developed a web-based interface for MREL Tool, and built a standalone API, as shown in Fig. 6.

Based on this model, two lifetime information was provided online to the test engineer: (a) under which test condition the stress is higher in the inverter system, (b) what is the current system-level reliability. Electro-thermal response for two different driving cycles were processed, i.e., WLTP and NEDC.

The rainflow counting plot in Fig. 7 illustrates the thermal cycling distribution across these driving cycles. For the WLTP mission profile, the MOSFET component in the inverter experienced the maximum number of cycles (5,800) at a mean junction temperature (T_{jmean}) of 80°C. In contrast, the NEDC cycle showed a slightly lower cycling count (5,500 cycles) at a mean temperature of 45°C, despite reduced temperature swings compared to WLTP, as visualized in the rainflow analysis. This discrepancy in temperature conditions is indicative of the WLTP's higher thermal stress due to broader temperature fluctuations compared to the less aggressive thermal profile in NEDC. Consequently, if we consider two mission profiles for the vehicle's operational lifetime — Mission 1 (M1): involving WLTP cycles exclusively, and Mission 2 (M2): consisting of a mix of WLTP and NEDC cycles — the expected lifetime for Mission 2 should be higher. This finding supports the validity of the assessment tool.

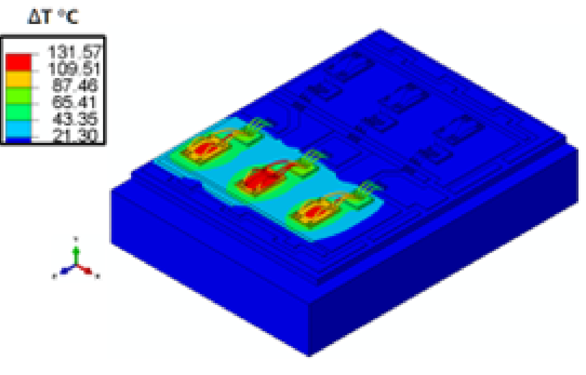
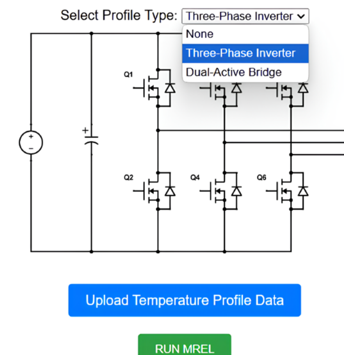


Fig. 5 Results of the thermo-mechanical simulation

MREL: Mission Profile oriented RELiability assessment tool



Upload Temperature Profile Data

RUN MREL

Fig. 6 Web-based MREL Tool for UC1c PHM activity

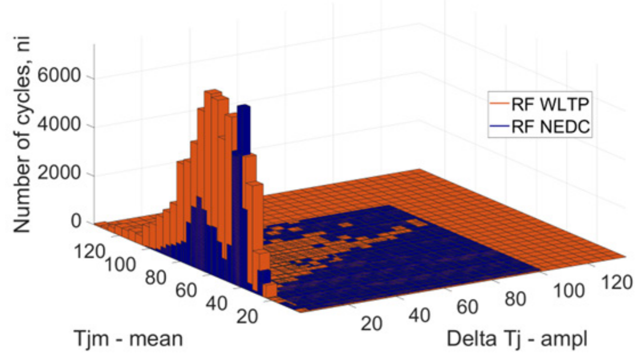


Fig. 7 Rainflow cycle counting results: Number of Cycles (ni), Mean junction temperature T_{jm} (°C) and Temperature swing Delta T_j (°C) for WLTP (orange) and NEDC (blue)

Fig. 8 presents the unreliability function (1 - reliability(x)) as a function of the distance covered by the automotive power converter (i.e., inverter) during M1 and M2 operations. It underscores that low/high side diodes contribute minimally to the overall system reliability. For instance, at the 99% reliability threshold, the inverter operating under M1 cycles achieve a reliable operational distance of up to 1,050 thousand kilometers, corresponding to a 1% failure rate, or 10 PPM. Under M2 operations, this reliable distance extends up to 1,750 thousand kilometers. Therefore, the physical phenomena observed in the individual thermal profiles of WLTP and NEDC are reflected in the overall system lifetime, with the inverter exhibiting extended lifetime under mixed driving cycles (M2) compared to WLTP-only cycles (M1).

However, it should be noted that the actual lifetime of the power converter is likely shorter than the predicted values shown in Fig. 8, as other failure-prone components (e.g., the DC-link capacitor, PCB, microcontroller, etc.) have not yet been considered in this framework.

IMPACT OF UC1C

UC1c demonstrated as a proof of concept a testing concept and setup to estimate the lifetime of power electronic components. This is done by using P-HIL testing of these components and combining it with simulation models for lifetime estimation.

Thereby, AVL-SET developed a P-HIL system, which can be utilized to record data from the unit under test, including critical parameters such as torque, duty cycle, temperature, and voltage, which enables a comprehensive analysis of the inverter's performance under standard driving cycles. This data, provided to the use case partners, plays a crucial role in assessing the durability and lifecycle of power electronic components. To estimate the lifetime of the individual components, very detailed simulation models, be it thermal or thermo-mechanical, are required. Thereby RWTH and TUC developed very advanced simulation models to be fed to a web-based lifetime assessment platform, coming from VUB. This "MREL Tool: Mission-profile-oriented reliability assessment tool" was further developed to be capable of investigating the impact of real-life mission profiles on automotive inverters, taking into account combined electro-thermal and thermomechanical fatigue. However, other failure-prone components (e.g., the DC-link capacitor, PCB, microcontroller, etc.) must also be considered within the framework to gain better confidence as future research.

By streamlining the lifetime testing of automotive power electronics, this collaborative approach establishes a cutting-edge reliability assessment methodology. It enhances collaboration among partners working on automotive reliability, reduces prototyping time, and positions each partner at the forefront of R&D in sustainable and durable automotive technology.

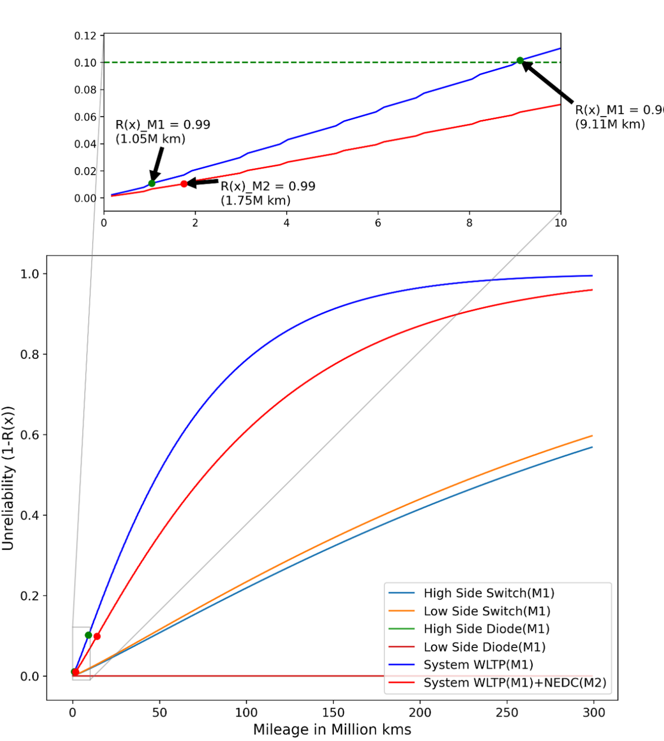


Fig. 8 The reliability of the system and active components (i.e., high and low side switch and diode) as a function of lifetime is shown, with the zoomed portion depicting reliability at 1% (i.e., 10 PPM) and 10% (i.e., 100 PPM) for M1 and M2 cycles, along with their corresponding mileage

UC1c Achievements

– Lifetime prediction (series failure rate) of power electronics systems (e.g., inverter) based on driving cycle-based load profile P-HIL testing paired with electrothermal and thermomechanical modelling and multi-physics simulation platform

UC2A

E-POWERTRAIN INVERTERS MULTIDRIVE E-POWERTRAIN

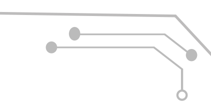
The primary objective of UC2a is to develop a modular, fail-operational traction inverter for electric vehicles. This inverter is designed to be scalable, reliable, and capable of safely handling both internal failures and external powertrain-level issues. The project focuses on enhancing component durability to extend operational life and ensuring integration with the vehicle's powertrain while meeting size and efficiency standards.

The main goal of UC2a is to create a traction inverter with a modular design and fail-operational capabilities, specifically designed for integration into the limited space and weight constraints of vehicles. UC2a aims to develop a modular inverter that can support driving multiple motors in a vehicle, with scalability to handle low and high power needs. The design must also ensure a fail-safe system, meaning that if the inverter experiences an internal failure, it will fail safely, and in the case of external vehicle powertrain-level failures, it will cooperate to shut the system down safely. Additionally, the inverter should be highly reliable, with an extended operational lifetime that requires no maintenance, achieved through research into the weakest components and ways to improve their durability. The modular inverter meets size and efficiency standards for next-generation electric vehicles, ensuring reliable, safe powertrain operation, advanced integration with the powertrain, and the ability to detect and respond to both internal and external faults.

RESULTS

In this use case, several partners collaborated to develop an innovative and smart multidrive unit. I&M, as the UC leader, played a central role in supporting the team throughout the entire design cycle, from defining requirements to testing physical samples. They contributed significantly to the design of several boards and sub-components, covering both electrical schematics and PCB layout. I&M also integrated these sub-components into the demonstrator and provided support to partners during the testing and validation phases. POLITO developed key models and control strategies, including: (1) circuital models for electrical machines (voltage behind reactance models) to study inverter faults, and (2) torque control strategies for three-phase and dual three-phase machines aimed at achieving high efficiency and fault-tolerant operation. TDK optimized the EMC filtering concept for the inverter based on pre-investigations. This ensured that an already refined

This UC was conducted in a collaboration of ten partners:
I&M, ELAPHE, IFAG, POLITO, TDK, TUC, TU/E, UNIPISA, VIF, VUB



The contributions of each partner are described as follows:

I&M (UC LEAD): design and prototyping of the multidrive unit demonstrator

ELAPHE: requirements definition and experimental validation at the test bed

IFAG: Silicon Carbide HybridPACK™ Drive Gen 2 module design

POLITO: circuital electrical machine models and torque control strategies

TDK: optimized EMC filtering concept

TUC: physics of failure based power module state of health estimation

TU/E: fast fault detection and reaction circuit

UNIPISA: real-time monitoring and ageing detection

VIF: data-driven based power module state of health estimation

VUB: cooling system design and optimization

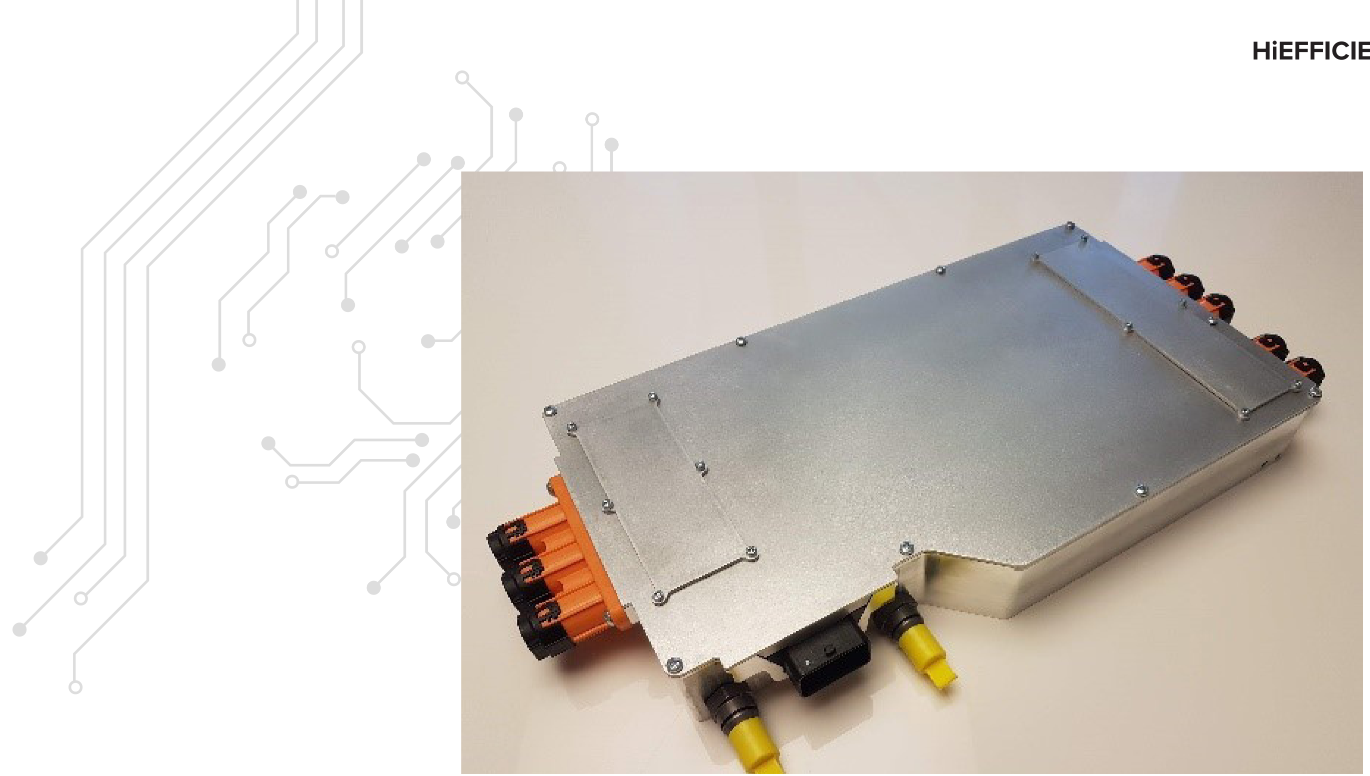


Fig. 1 Multidrive Inverter

EMC filtering approach was implemented when the new inverter hardware became available. TU/e developed a method capable of detecting and mitigating a shoot-through-like short circuit event in less than 200 ns, fast enough to protect the power module from damage. They also created analytical models to account for parasitic elements during short-circuit events, using these models to optimize the detection method. VIF focused on Prognostics and Health Management (PHM) related to the dual inverter, using a reliable State of Health (SoH) estimation method based on Data-Driven (DD) models. Since data from accelerated aging tests was limited, synthetic data was generated using a MATLAB Simulink-based electro-thermal model. This data was used to train Deep Neural Networks (DNN) (including CNNs and LSTMs) to estimate the SoH of SiC MOSFETs, which facilitated predictive maintenance. Initial results showed SoH estimates above 80%, decreasing below 10% as degradation increased. Furthermore, in collaboration with TUC they integrated Physics of Failure (PoF) and data-driven approaches into a hybrid estimation method. TUC focused on developing a PoF-based methodology to assess the health state of SiC power modules by analysing their mechanical behaviour. High-fidelity finite element simulations were carried out, but due to their computational complexity, a surrogate model was developed for practical implementation. This surrogate model is the first of its kind to capture the nonlinear, health-dependent mechanical behaviour of power electronic modules under switching conditions. VUB investigated different cooling concepts, including serial and parallel configurations, to enhance thermal management and uniform cooling efficiency for the UC2a dual inverter applications using Infineon's 1200 V SiC MOSFETs (CoolSiC™) within HybridPACK™ Drive modules featuring a pin-fin base plate. The cooler structure design was optimized through a systematic iterative design cycle, starting from CAD modelling and progressing through CFD simulations, as shown in Fig. 2, to evaluate thermal performance. The final cold plate design underwent extensive CFD simulation analysis under diverse conditions, while evaluating its thermal performance, before being implemented in the dual inverter prototype for experimental validation tests. These contributions by the various partners were crucial to conceive, design, build, and test an integrated smart multidrive unit. Parallel to the development of a smart modular electric drive system, prognostic and health management and functional safety (FuSa) analysis has been conducted with the goal to identify possible faults on the inverter over its lifetime. Therefore, a Hazard Analysis and Risk Assessment (HARA) and Failure Modes and Effects

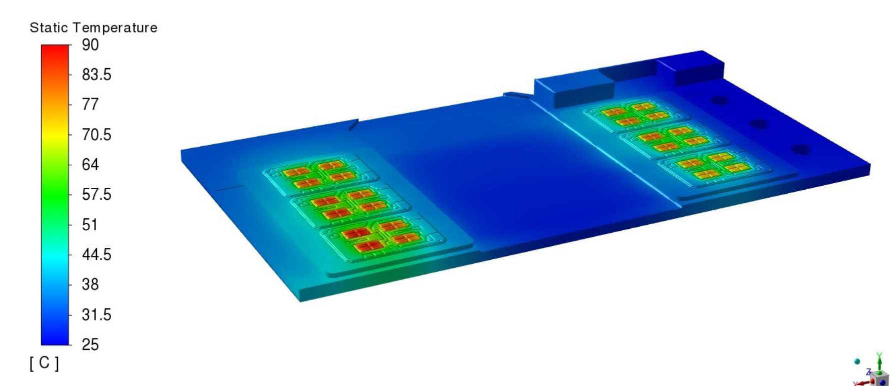


Fig. 2 CFD Simulation of the Dual Inverter

Analysis (FMEA) has been completed. The potential risks identified served as baseline for prognostic and health management. This workflow is devised in accordance with ISO 26262 in the context of a target vehicle application. The result is a compact unit able to drive up to two motors for a total output power in the range of 500 kW occupying a volume of 7.5 liters, including power connections and EMC filters. The unit provides a power density close to 70 kW/l which is an outstanding value in the 400 V battery voltage range.

The unit features advanced virtual sensing solutions to monitor power stage temperature and electrical performances. These data, together with application-dependant parameters collected in real-time, serve as input for the compact surrogate models (either DD or PoF-based methodologies) developed to estimate the remaining useful life of the unit.

IMPACT OF UC2A

UC2a delivered significant results towards all project objectives. An innovative design process heavily supported by multi-physical, multiscale simulation platform was developed along the project. In this approach the same simplified digital twin models used offline during the concept/design phase are then used to generate embedded observers able to estimate critical real-time parameters during the operational life of the unit. This includes parameters related to the estimation of the remaining useful life. To capitalize on the outcomes of UC2a, we are currently assessing the technology innovations developed throughout this project to plan their integration into I&M's motor controller's product line. From the hardware perspective, SiC module HybridPACK™ Drive Gen2 are backward compatible with existing motor controller housing, so the upgrade is quite straightforward, resulting in improved power density and efficiency. In terms software, aligning with the growing demand for intelligent, durable, and resource-efficient solutions, the plan is to embed the mentioned monitoring capabilities into existing controllers. I&M will focus first on thermal aspects: improving monitoring capabilities on SiC junction temperature. This will enhance the efficiency, reliability, and longevity of current products. As second step, this also opens opportunities to develop a new generation of market-ready products that offer predictive maintenance and real-time performance insights. Ultimately, these advancements will provide customers with more reliable products and contribute to the wider adoption of sustainable technologies, benefiting both industry stakeholders and the public through improved energy efficiency and reduced maintenance costs.

Fig. 3 Detailed simulation model for the electro-thermo-mechanical simulation in order to assess the mechanical behaviour

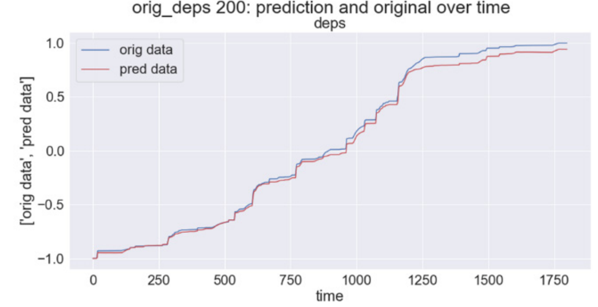


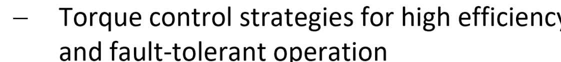
Fig. 4 Prediction accuracy of the developed surrogate model for predicting the damage state

Cooling system design and optimization studies at VUB have generated key insights into advanced cooling solutions for electric vehicle traction inverters. The resulting methodologies and knowledge base for optimizing cooling systems will be leveraged and expanded in ongoing and future research, advancing VUB's work in cutting-edge thermal management.

UC2a Achievements

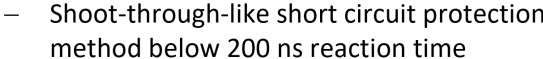
- 40% power density increase compared to baseline achieving 70 kW/l, including EMC filters

- Efficiency >98% for most operating points using different PWM



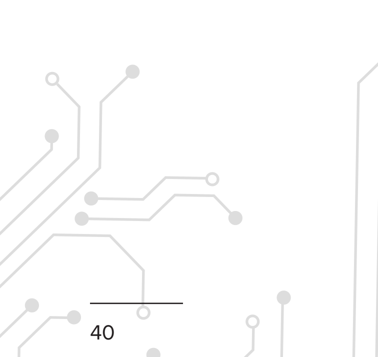
- Torque control strategies for high efficiency and fault-tolerant operation

- Hybrid DD and PoF PHM approach



- Shoot-through-like short circuit protection method below 200 ns reaction time

- SiC junction temperature observer



UC2B

E-POWERTRAIN INVERTERS HIGHLY INTEGRATED E-POWERTRAIN

Wide-bandgap semiconductors are crucial for electrification in transportation, which has been demonstrated already in different applications. They offer higher power densities, less waste heat, higher voltage levels, and longer lifespans. SiC is widely used in automotive power conversion, while GaN is prevalent in mobile phones. To unlock GaN's full potential, technical improvements on integration are needed. Embedding GaN SoC in PCB reduces stray inductances, optimizing switching and minimizing losses. This is in focus of this use case to demonstrate the potential advances.

The goal of UC2b is to develop a modular inverter leg using 650 V GaN half-bridge SoC devices embedded within a PCB. The key objectives include minimizing the overall size and reducing parasitic effects of the GaN-based power module through chip-embedding technology. An „on-demand" modular approach has been explored, allowing the parallelization of dies or legs based on specific application needs to maintain high efficiency across the power range. The design also features a variable switching frequency of up to 50 kHz to optimize efficiency, aiming to meet or exceed 98%. Additionally, the reliability of the module has been investigated at lab level.

RESULTS

Several partners made significant contributions to the UC2b developments. As the UC Leader, I&M guided the design process from requirements definition through to testing physical samples. They designed the electrical schematics and PCB layout for two learning cycle boards, which were integrated into the power stage demonstrator. Further, AT&S played a key role in the embedding and packaging of the system-on-chips (SoCs) developed by imec. They also supported the design of half-bridge modules with embedding technology, fabricating the modules designed by I&M. The first iteration of modules used discrete GaN HEMTs for embedding and AT&S performed a static characterization of those. Additionally, the provided insights into sinter technology were crucial for mounting the half-bridge modules onto the cooler. Imec was responsible for the design of the 650 V SoC devices and contributed to discussions on the topologies, IOs, and the selection of the chips. They SoCs have been thoroughly tested with respect to functionality to gather inputs for improvement in a second learning cycle. MBAG supported the project by conducting thermal and electrical characterizations of the half-bridges with embedded GaN chips. These tests, conducted on both aged and unaged modules, allowed for an assessment of the lifetime of the modules. Additionally, a GaN inverter was built to test the performance of GaN on a machine test bench, demonstrating its suitability for the use in a traction inverter. Electric-thermal and thermo-mechanical simulations of power mo-

This UC was conducted in a collaboration of six partners:
I&M, AT&S, IMEC, MBAG, TUC, SAL

The contributions of each partner are described as follows:

I&M (UC LEAD): design and prototyping of the multidrive unit demonstrator

AT&S: manufacturing and test of the half-bridge modules with embedded dies

IMEC: design and manufacturing of the GaN SoC 650V

MBAG: requirements definition and test bench validation

SAL: thermal and mechanical simulation analysis

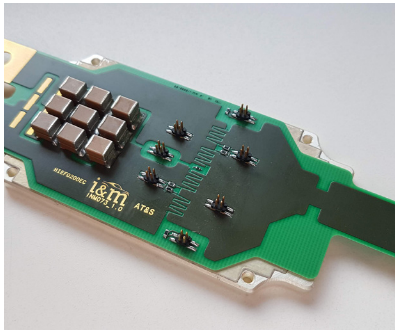
TUC: thermo-mechanical simulations and power cycle testing

dules to assess their mechanical robustness have been carried out by TUC. They also performed power cycle tests and physical failure analysis on the first learning cycles to study the stress effects on the power module. SAL focused on thermal and mechanical simulations of the power electronics embedded packaging concepts for a three-phase traction inverter system. They evaluated packaging designs from two learning cycles: one using discrete GaN dies and the other incorporating GaN half-bridge SoCs. SAL also developed reduced-order thermal models for rapid electrothermal simulations, which were key in assessing the reliability and performance of the power devices and packages under various operational scenarios. This included also simulations on an optimal temperature sensor location to secure a safe operation (Fig. 1 right). This coordinated effort between the partners resulted in a comprehensive exploration of power module design, testing, and simulation for high-performance automotive applications.

The results confirm blend benefits of embedding power element technology and GaN devices. With this demonstrator, the embedding technology is the key enabler for a PCB layout aimed at reducing the stray inductance: this is the necessary condition to fully exploit the superior switching frequency performances of GaN devices. Stray inductances in the range of 9.1 nH to 3.4 nH – depending on the capacitors configuration – were measured. It needs to be further highlighted that outstanding results in terms of reliability have been achieved. More than 4500 thermal shock test cycles according to AQG34 specifications have been performed with zero defect.

IMPACT OF UC2B

This use case demonstrates that Gallium Nitride materials in combination with PCB embedding technology represent a solid alternative to Silicon Carbide also in high-voltage (450 V) medium power applications (few tens kW). This technology enables higher switching frequency operations, therefore the benefits of lowering the Total Harmonic Distortion (THD) of the motor phase currents can be investigated. Additionally, the developed units show remarkable reliability features, which have been confirmed by power cycle tests (FIg. 2 and Fig. 3). The according experimental procedure for testing such modules was developed to enable reliability testing of future embedded GaN power modules. The suitable temperature range was investigated, still within a reasonable range to avoid shifting of the failure mechanisms but ensuring short test times. This still remains a challenge for the future. However, the test results show a great potential of the embedding technology to achieve highly reliable GaN power modules and making this solution suitable for future automotive powertrains.



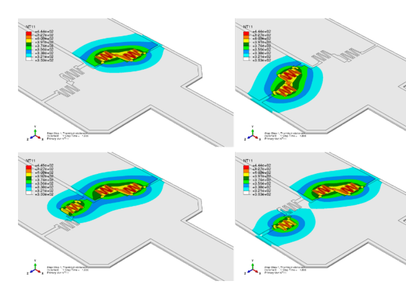


Fig. 1 650 V GaN SoC half-bridge module (left) and electric-thermal simulation results to identify best temperature senor position (right)

Test parameter	Value
Colling	Cooling plate
Messparameter	U_F, P_V, $T_{j,min}$, $T_{j,max}$, $R_{th,j-c}$, T_h, I_G, Z_{th}, ...
Test strategy	const. Test parameter (t_{on}, t_{off}, I_L = const.)
Parameters	$U_{GS,on}$ = 5V ; I_{sense} = 3A
Failure criteria	+5% $V_{CE,sat}$ / +20% $R_{th,j-c}$ / Function failure

	Test 1
$T_{j,min}$ [°C]	10
$T_{j,max}$ [°C]	150
$\Delta T_{j,APC}$ [K]	140
t_{on} / t_{off} [s]	3 / 6

Fig. 2 Power cycle test parameters

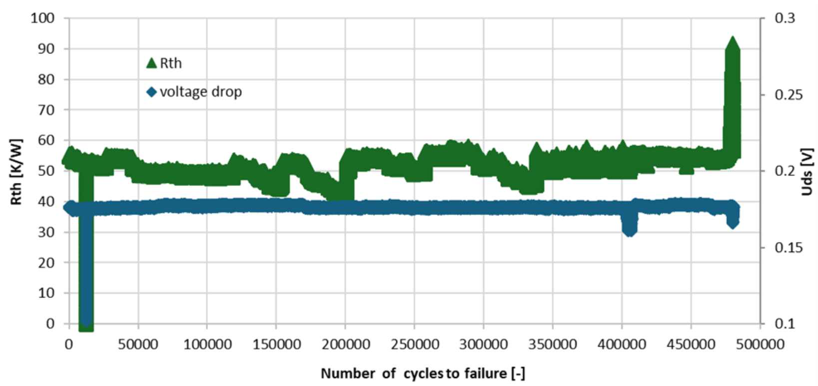


Fig. 3 Power cycle test results of 1st iteration UC2b power modules

UC2b Achievements

– Highly compact high-voltage GaN based half bridge module

– Highly reliable power modules, withstanding 4500 thermal shock cycles and 490,000 power cycles with high dT

– Temperature sensors closest to the active area
– Voltage level shifter integrated close to the die

UC3

HIGH POWER 48 V DC/AC INVERTER

The goal of UC3 is to create a compact automotive traction inverter with a 48 V battery voltage. The inverter's power stage uses embedded GaN dies in the PCB, which enhance mechanical stability and thermal performance. WBG semiconductors improve switching and thermal performance, as well as extending the lifespan. With the power switches embedded in the PCB, the entire bottom surface can serve as a coolant interface, maximizing cooling efficiency. The modular design of the commutation cell allows for scalability and adaptability based on application requirements.

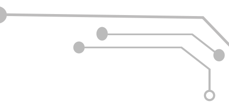
The scope of UC3 is the development of a highly compact automotive traction inverter targeting a 48 V battery voltage. The power stage of the inverter uses embedded GaN dies in the PCB. Embedded die packaging not only brings design flexibility but also provides high mechanical stability and better thermal performance. WBG semiconductors have better switching performance, and they also provide better thermal performance and longer lifetime. As the power switches are already embedded into the inner layers of the PCB, there is no component at the bottom side of the PCB. Hence it is possible to use the complete bottom surface of the power module as a coolant surface. The isolated bottom surface of power modules allows to place them directly on the cooler to have best cooling performance. The commutation cell is designed in a modular way to scale the design according to requirements and to replace the subparts based on the application.

RESULTS

To realize the 48 V inverter, two versions of the power module have been developed and manufactured with different bare die GaN switches. The first power module version has 80 V and 180 Arms voltage and continuous current ratings respectively. The second power module is rated at 100 V and 180 Arms (Fig. 1). The power modules are using bare dies being embedded in the PCB. This brings a significant advantage in volume, reducing the volume by 18.75% compared to SMD GaN switch-based power module. The comparison has been made by taking an SMD test board design as a reference and by considering top side cooling requirement of SMD switches. Both designs have GaN switches with same current capability.

To achieve the desired power values, three half-bridge modules are put in parallel per phase, having in total 9 half-bridge modules in the inverter. The maximum current of three parallel power mo-

This UC was conducted in a collaboration of nine partners:
AVL-SFR, AT&S, FORD, MBAG , RWTH, TDK, TUC, VIF, VUB



The contributions of each partner are described as follows:

AVL-SFR (UC LEAD): took care about the overall inverter system and development and testing of the inverter-hardware

AT&S: manufacturing of the half-bridge modules with embedded dies

FORD: proposed and defined system architectures and requirements for the hardware

MBAG: static and dynamic characterization tests of the manufactured power modules

RWTH: thermal model of the power module to analyse temperature distribution and optimize sensor placement in future generations of the power module

TDK: filter-design and EMC concepts of the inverter

TUC: tests and analysed state of the health parameters

VIF: cooling simulations and cooling concepts

VUB: electric simulations for half-bridge modules to find the most efficient design solution

dules was measured as 840 A during double pulse testing of the modules. This is in line with having two high side and two low side power switches with 140 A peak current rating in one power module and having 3 modules in parallel.

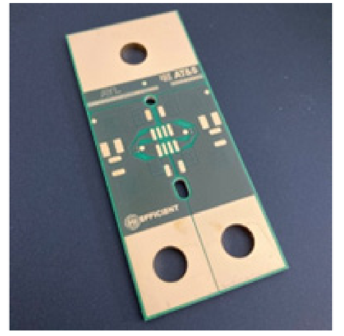
The measured switching losses during double pulse tests were used as inputs for efficiency simulations (Fig. 2 and Fig. 3). Based on these values the efficiency of the inverter was calculated to be over 98%.

Since new approaches for embedding bare dies in the PCB have been followed, e.g. sinter lamination with Cu-paste (cf. also key results section on the integration methodologies), thorough testing of these modules have been performed. Therefore, failure modes of UC3 power modules with embedded dies (80 V / 180 A) under power cycle conditions and corresponding effects of ageing on electrical parameters were analysed.

A very high lifetime of 290,000 cycles under power cycle conditions was observed for one module under harsh loading conditions (dT=140°C). Test conditions are given in the Fig. 4. The cycle results are shown in Fig. 5, where a peak is visible at the end of the cycle and thus the test stopped.

Further, both power module variants (80 V and 100 V) of the half-bridge modules were reliability tested according to AQG324. For the first version of the power module (80 V dies), end-of-life test have been performed, which means testing until failure. Contrary, the test for the second variant (100 V dies) have been stopped after 2000 cycles and hours respectively. For both variants, the tests as proposed by AQG324 could be completed successfully. To see the limitations, in case of variant 1, end of life was just achieved after 2870 hours of testing in case of HTGB, HTRB, HTS, and H3TRB testing. Thermal Shock Testing (T_{min}=-55°C, T_{max}=175°C) showed after 1500 cycles only 50% of failed modules so the test was extended to 2000 cycles which is 1360 cycles above the minimum requirement for passing the test. Based on the learning of variant 1, further improvements have been made in the development of the second variant, leading to even more stable modules in the course of testing. Summarized it becomes evident that both variants show very stable power modules.

The mechanical parts of the inverter were designed in a modular approach. The power density of the commutation cell (including control board, gate driver board, power modules, busbars, DC link and power module carrier which is the main structure element of inverter) is calculated as 44 kW/l and hence improving by more



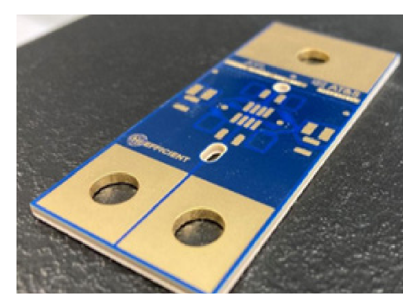


Fig. 1 Manufactured half-bridge modules with 80 V (left) and 100 V GaN (right) dies

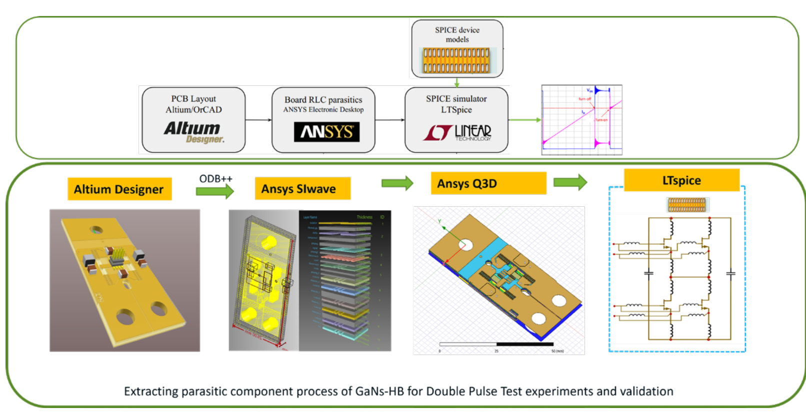


Fig. 2 Procedure for investigating switching performance of GaNs HB modules and extracting parasitic components in the embedded dies PCB structure for accurate system simulation and configuration

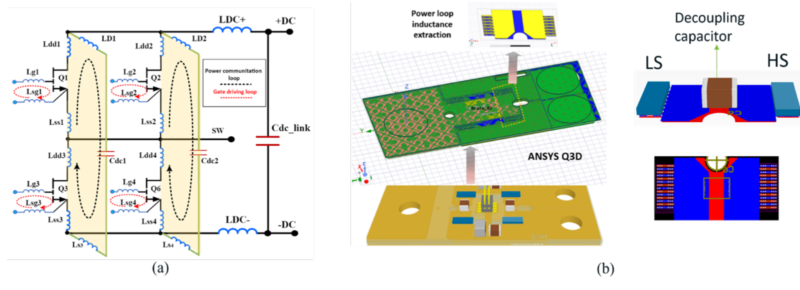


Fig. 3 Circuit equivalent model with parasitic inductances. Parasitic components in PCB embedding structure: (a) parasitic inductance distribution circuit, (b) PCB configuration and analysis

Test parameter	Value
Colling	Cooling plate
Messparameter	U_F, P_V, $T_{j,min}$, $T_{j,max}$, $R_{th,j-c}$, T_h, I_G, Z_{th}, ...
Test strategy	const. Test parameter (t_{on}, t_{off}, I_L = const.)
Parameters	$U_{GS,on}$ = 5V ; I_{sense} = 3A
Failure criteria	+5% $V_{CE,sat}$ / +20% $R_{th,j-c}$ / Function failure

	Test 1
$T_{j,min}$ [°C]	10
$T_{j,max}$ [°C]	150
$\Delta T_{j,APC}$ [K]	140
t_{on} / t_{off} [s]	3 / 6

Fig. 4 Test conditions for power cycle testing

than 45% compared to the baseline. Analysing the impact of the power switching events on signal integrity by the board layout in advance helped to achieve a compact design without functional risks (Fig. 6). Therefore, the electrical parasitics of the board layout had been implemented into a simulation model to analyse the impact on signal integrity and an optimization process followed.

CFD simulations were performed for investigating the cooling performance of the inverter. This was achieved by using surface enhancing structures (pin-fins) which increase the cooling capacity. The inverter's power module acts as the heat source. To assess cooling performance, the temperature gradient is calculated across the module's material layers, designed to absorb heat from the dies. With top-side cooling, this setup keeps the inverter below critical temperatures, preventing failure. Simulations were conducted using OpenFOAM with the ‚chtMultiRegionSimpleFoam' solver for three cases with inlet flow rates of 10 l/min, 8 l/min, and 6 l/min. Fig. 7 shows temperature contours of the main body (for the best case of 8 l/min). The coolant effectively absorbs heat from the first source, but its efficiency decreases as it moves forward, leaving the third heat source hotter than the first. Notably, the temperature difference between the first and second sources is only 30°C.

Finally, the inverter was integrated including all relevant components (Fig. 8) and underwent P-HIL testing to verify the envisaged targets. The GaN based 48 V inverter has been tested up to 100 A RMS and 5.8 kW output power at P-HiL within the project duration. The simulated efficiency was over than 98% for the inverter and 97% system efficiency measured during the tests. The difference between the measured and simulated efficiency is caused by the system environment such as cable connections. Looking on all set requirements, most of the objectives in this use case have been achieved

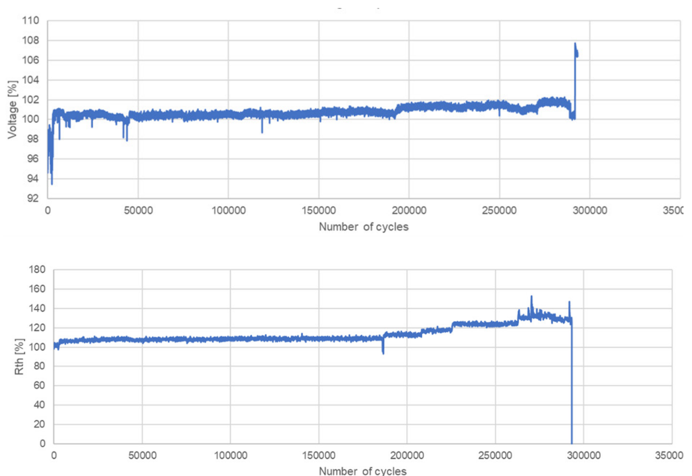


Fig. 5 Voltage drop under power cycle test condition for 80 V GaN dies (top) and thermal resistance under power cycle test condition for 80 V GaN dies (bottom)

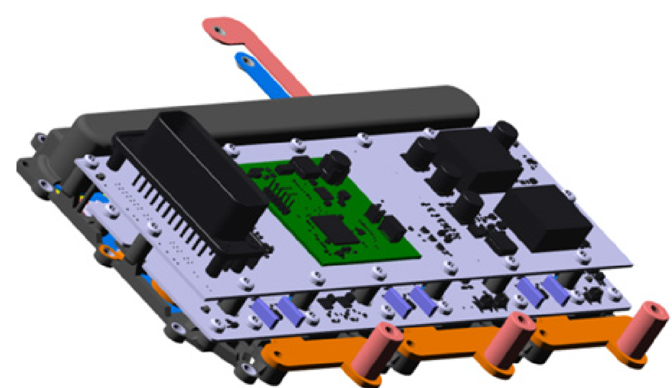


Fig. 6 Commutation cell

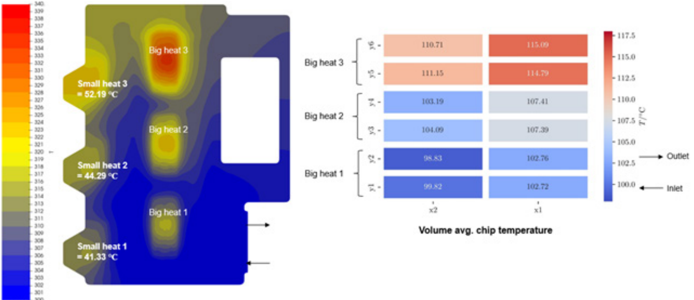


Fig. 7 Temperature contour of the main body, volume averaged die temperature (8 l/min case)

IMPACT OF UC3

Every weight reduction is beneficial for electric cars to be able to provide more range to drivers. Increased power density will be extending the range of electric cars further. Usage of WBG semiconductors and bare die technology will be more common in automotive applications as they bring system compactness and more efficiency. The lessons learnt from the development and testing stages are contributing special know-how to each stakeholder.

The 48 V inverter prototype with embedded GaN dies, in-house designed control and driver circuit was developed by AVL-SFR, which can be also scaled to HV applications. With the gained know-how, AVL-SFR is ready for tailoring the inverter according to market demands with the help of modular mechanical design.

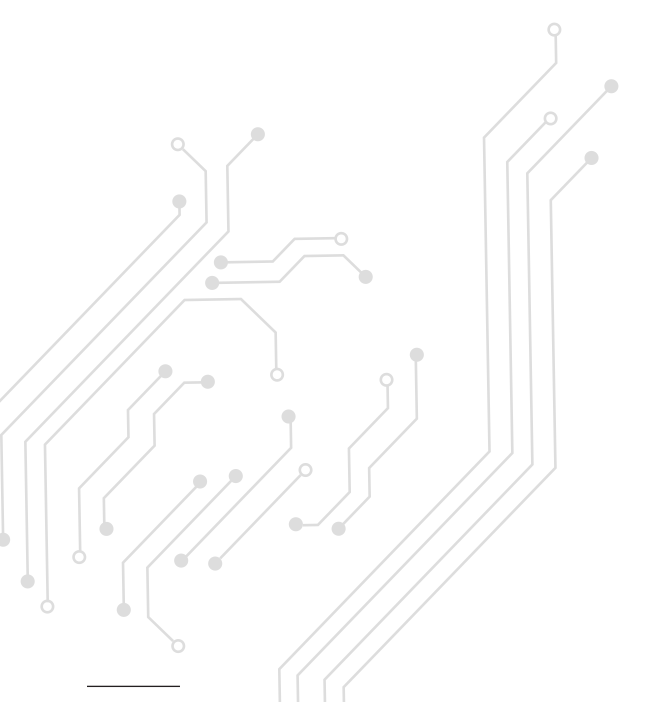
VUB has developed multi-physics simulation models of Gallium Nitride (GaN) power semiconductors to evaluate their potential for handling high peak currents, fast dynamics, parallelization, and thermal dissipation in next-generation high-power traction inverters for low-voltage applications. VUB's contributions include the determination of the parasitic power loop inductances and circuit simulations of parallel power module configurations in LTspice to support module and inverter prototypes' design and testing in an iterative approach. In addition, optimizing gate resistor implementation during ON and OFF states, improving switching behaviour, and evaluating switching losses (Eon/Eoff) and inverter efficiency under various conditions are used to refine the design process and provide valuable guidelines for the early stages of GaN-based inverter design. These insights strengthen VUB's expertise in advanced GaN technologies and will support future industrial and academic projects.

MBAG has investigated the performance of GaN and embedding in UC3. It has been proven that it is possible to build compact power modules with low stray inductance using embedding technology and to integrate GaN into them. The lifetime was examined. This

Fig. 8 Integrated inverter prototype

knowledge can be utilized by MBAG to incorporate it into future power electronic designs.

The thermal shock and power cycle tests confirmed the great potential of the embedding technology to achieve highly reliable GaN power modules. On the TUC side, the experimental procedure for testing such modules was developed to enable future reliability testing of embedded GaN power modules. The suitable temperature range was investigated, still within a reasonable range to avoid shifting of the failure mechanism but ensuring short test times.



UC3 Achievements

– 46% power density increase achieving 44 kW/l by using GaN switches and power electronics embedding

– Efficiency of 99.2% at 59 Arms and 98.2% at 538 Arms

– Advanced power cycling test setup for embedded power modules

UC4

MULTI-USE DC CHARGERS

Addressing the increasing demands of e-mobility, particularly for fast DC charging, UC4 focused on the development of a charging system featuring dynamic reconfiguration of multiple grid-isolated Power Conversion Modules (PCMs). Thereby, the focus is on an advanced power electronic converter system — efficient, reliable, reconfigurable, and highly integrated — using modular PCMs equipped with SiC power devices. By isolating the functionalities of power conversion, dynamic power routing, and DC connection and communication within the charging system, the design allows for separating the number of power conversion units from the number of charging posts where EVs connect. Consequently, EVs can be queued while maintaining active communication with each one. Conversely, the system can also deploy multiple PCMs in parallel to supply power to a single EV.

The proposed converter system is designed to meet diverse charging requirements for different e-mobility devices. Moreover, the flexibility of the charging infrastructure will be enhanced through the development and testing of new charging functionalities. These functionalities are intended to operate independently of the performance levels and specifications of the PCMs.

In UC4, a highly efficient and reliable Power Conversion Module (PCM) that forms the building blocks of a DC charger has been developed by Heliox (Fig. 1). This PCM adopt a two-stage design. It includes a T-Type converter as the Active-Front-End (AFE) and a derivative of the Dual-Active-Bridge (DAB) converter which provides galvanic isolation and output voltage and current regulation. The PCM developed in the project had an efficiency target of 97%.

VUB supported the selection of converter components, control algorithm design, and cooling system design with a strong focus on reliability. Thermal validations were conducted to optimize cooling performance, ensuring robust thermal management. Additionally, a dedicated Predictive Health Management (PHM) circuit was implemented to continuously monitor lifetime-sensitive parameters. These data were analyzed in real-time to actively adjust converter operation, thereby extending the system's operational lifespan.

In addition, partner TU/e built a three-phase isolated series-resonant AC/DC converter. It offers direct conversion from AC to DC, which reduces costs and increases power density. The team from TUDO built a gate driver network that maximizes the switching transient and reduces overshoots and rings in switches. The team from TNO came up with an algorithm which exploits the high switching frequency of DC charger based on SiC switches. This algorithm performs Electrochemical Impedance Spectroscopy (EIS) of a battery which gives information of battery cell internal resistance and cell temperature.

This UC was conducted in a collaboration of six partners:
HELIOX, IFAG, TNO, TUDO, TU/E, VUB

The contributions of each partner are described as follows:

HELIOX (UC LEAD): prototyping of power conversion module and facilitating charger integration

IFAG: double-side-cooled SiC half-bridge module and gate driver chip

TNO and **TU/E**: estimating internal battery temperatures by modifying the output current profile of a WBG charger

TUDO: gate driver network improving switching transient and reducing switching overshoot

TU/E: series-resonant converter that offers direct conversion from AC to DC

VUB: control/modulation strategy, cooling system design, validation of converter operations, and PHM / Design for Realibility (DfR) of converters

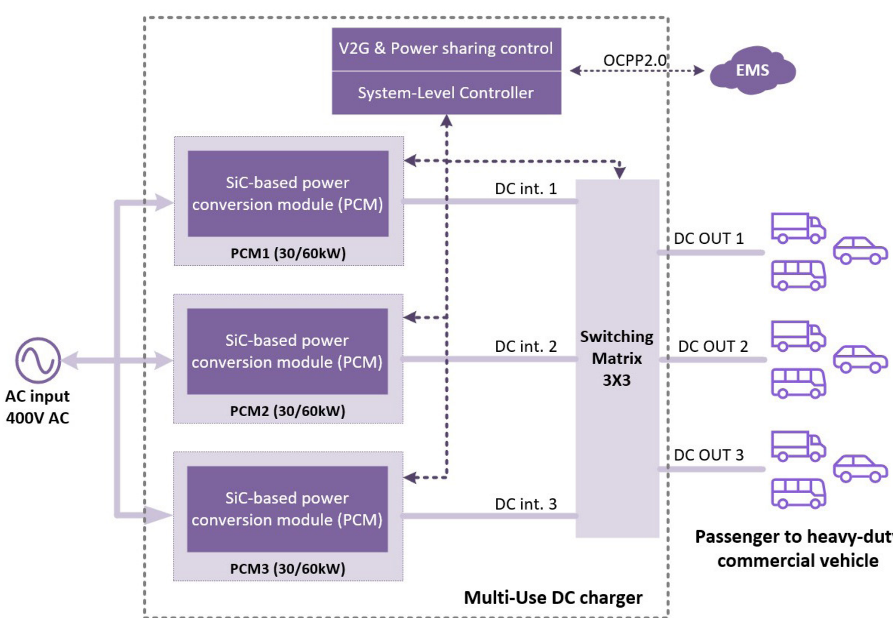
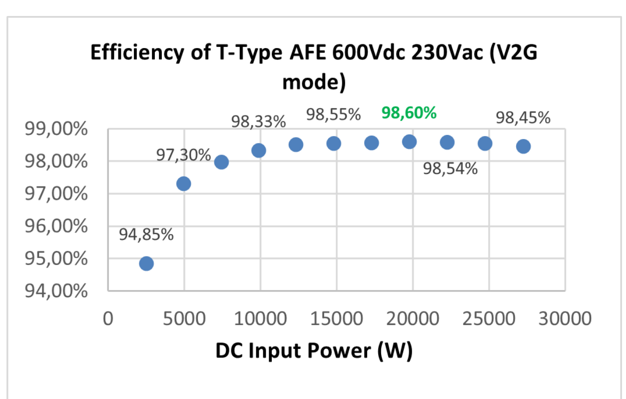


Fig. 1 Architecture of multi-use DC charger in UC4

RESULTS

A wide-bandgap based power conversion module has been developed in this project. Due to the employment of SiC switches and multi-level topology in the AFE design, the volume of filter is reduced by 13%. In addition, the conversion efficiency of the AFE is also boosted to 98.6% peak efficiency in V2G mode and 98.5% peak efficiency in charging mode, as shown in Fig. 2. Fig. 3 shows the 30 kW T-Type AFE. It adopts 3rd gen SiC 1.2 kV 21 mΩ MOSFET for the leg switch, and 3rd gen SiC 650 V 25 mΩ MOSFET for the neutral switch. The copper thickness of the PCB is only 70 µm. A heatsink with dimension of 140 mm * 210 mm * 20 mm and a fan operating at 6 W is sufficient to dissipate the heat from those switches. The junction of all switches is maintained less than 91 degree @ 27 kW operation.

At the beginning of the project, 4th gen SiC were not available and the low $R_{ds,on}$ offered poor performance price ratio. However, for the past three years, price of SiC MOSFET is dropping, and the 4th gen switches is publicly available. It is expected that the efficiency of AFE will increase further by adopting thick PCB prototype and 3rd gen SiC 650 V 15 mΩ MOSFET for the neutral switches and 4th gen SiC 1.2 kV 18 mΩ MOSFET for leg switches.



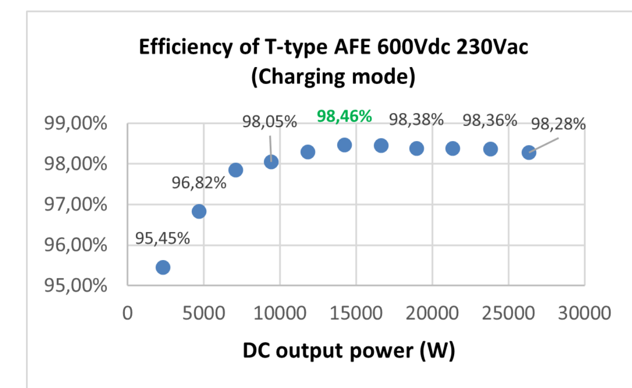


Fig. 2 Efficiency curve of T-Type AFE running in V2G mode and charging mode

Fig. 3 30 kW T-Type AFE

A DSC-based DAB demonstration has been developed to provide 30 kW output power under full load conditions, as shown in Fig. 4. It consists of 4 Infineon FF06MR12A04MA2 DSC switches, 2 relays to change the turns ratio, an auxiliary inductor, a tap transformer and DC-link capacitors on both the input and output side. To evaluate the cooling performance of the system, the thermal resistance from the heat sink to the junction has been calculated using Computational Fluid Dynamics (CFD) simulation in Ansys Fluent, as shown in Fig. 5. This thermal resistance was further verified by experimental tests using thermal imaging.

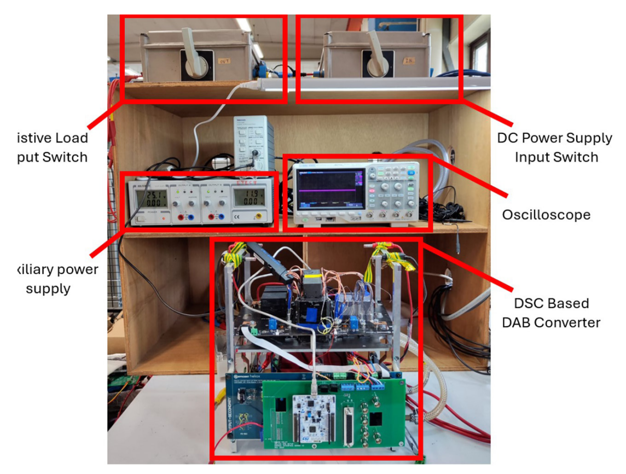


Fig. 4 DSC-based DAB converter test setup

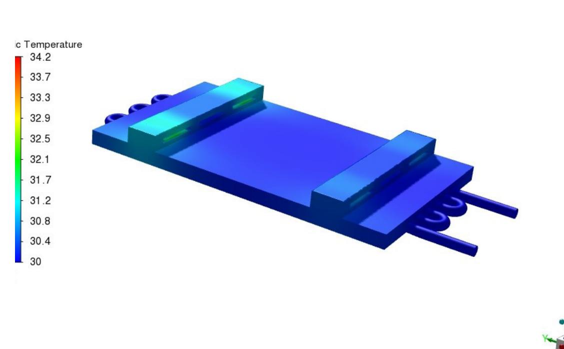


Fig. 5 DSC-based DAB converter thermal CFD simulation of the converter heatsink

In UC4, the PHM circuit was developed to measure on-state voltage and current while incorporating noise removal techniques and correcting the correlation between voltage and current, as shown in Fig. 6. This measurement is achieved by triggering the PHM circuit at specific moments to capture only the necessary data, avoiding extraneous information. The circuit is designed to measure the drain-source resistance ($R_{ds,on}$). Following the design phase, initial and final testing of the PHM circuit were conducted.

The output results indicate that the measured $R_{ds,on}$ can effectively track changes in junction temperature by adjusting the output load, as shown in Fig. 7. Therefore, $R_{ds,on}$ shows significant potential as a precursor in the PHM methodology.

Fig. 6 PHM circuit of DSC-based DAB converter

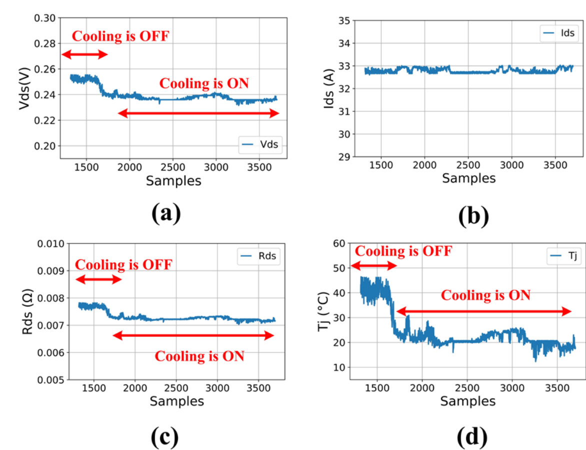


Fig. 7 DSC-based DAB converter measured signals through the PHM circuit: (a) drain-source on-state voltage; (b) drain-source current; (c) drain-source resistance; and (d) junction temperature

Contrary to the usual AFE-DAB topology, a scaled prototype of a series-resonant AC/DC converter-based charger was developed, as shown in (Fig. 8). This is intended for small electrical vehicles. The developed switching methods allow to reduce the steepness of switching voltages (dv/dt) to almost any desired (low) level, regardless of the internal switching speed of the semiconductors themselves. As a result, electromagnetic emissions are expected to be much reduced, which allows the associated filter components to be smaller and less costly than for the state of the art. At the same time, grid-side currents at a high power factor and with low distortion are achieved.

Thanks to the WBG based chargers, there is more freedom to shape the charging current profile. TNO and TU/e collaborated to investigate battery Electrochemical Impedance Spectroscopy (EIS), which is the frequency response diagram of the battery. This provides the cell impedance which is correlated to the internal cell temperature.

Fig. 9 shows the test set up in TNO, a custom-made WBG-based charger developed by TU/e excites a series of sinusoidal current signals ranging from mHz to 10 kHz. Battery voltage information is then logged to derive the EIS diagram, which is used to estimate cell temperature.

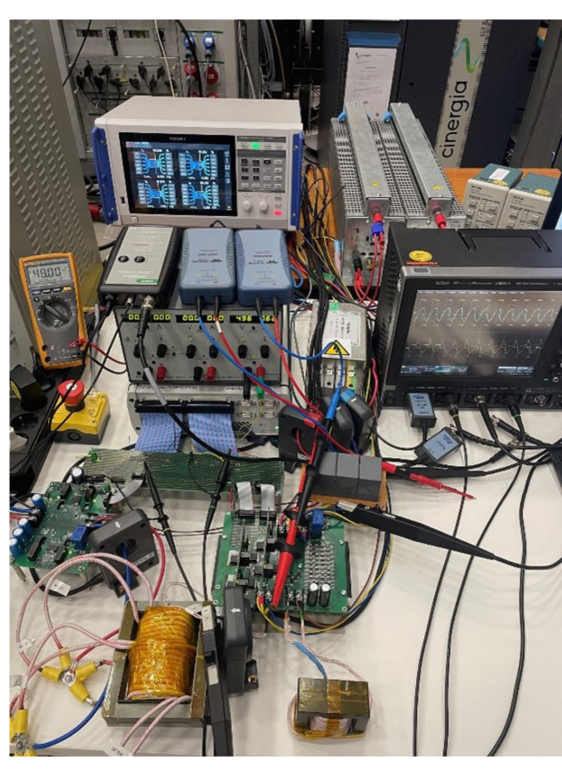


Fig. 8 Test setup of series resonant AC/DC converter

Fig. 9 Test setup of battery EIS

Experimental results show that the estimated cell temperature is within 3 degrees of the actual temperature.

A three-level gate driver network was developed in the project, as shown in Fig. 10. It implements a gate driver circuit that does not affect the gate driver IC and the SiC power semiconductor, either in a discrete package or as a module. The Active Gate Driver (AGD) implements a variable gate resistance during the switching transient of the semiconductor, effectively influencing the switching transient. It enables faster transient and reduces ringing of SiC MOSFET. This leads to reduced switching loss by 7.8% to 15.9% depending on the gate resistance of the reference gate driver. This allows a high frequency switching of the application and increases the power density of the system. In addition, the EMI has not increased despite the faster switching transient.

IMPACT OF UC4

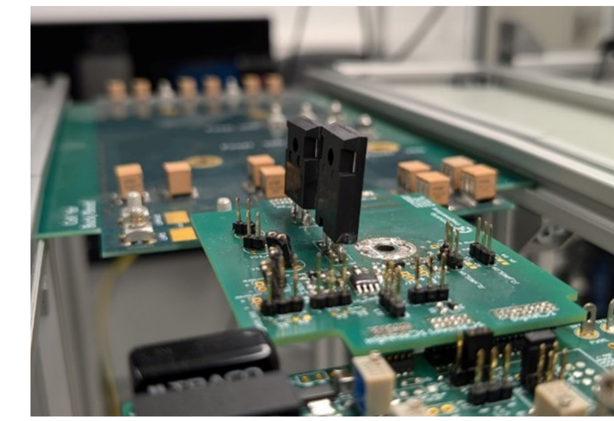


Fig. 10 PCB of three-level active gate driver and its double-pulse

As the market is getting more and more competitive and customers are seeking to lower operation costs, maintaining the industry leading high-power depot-charging business is more challenging than ever before. The technical how-know accumulated in this project, especially the proven concept of using SiC switches and 3-level and DAB topology to achieve smaller volume and higher efficiency gives Heliox a jump start on developing next-generation efficient and reliable high-power chargers. This will help Heliox maintain the market position in the long term.

VUB has introduced an innovative power electronics optimization approach, incorporating „Design for Reliability (DfR)“ to enhance system efficiency, reduce size, and extend the lifespan for both AC/DC and DC/DC stages in UC4. Intelligent low-level control strategies for the DC/DC stage, validated through hardware prototype, achieved an impressive 98.2% efficiency at maximum load. Additionally, VUB developed an in-situ $R_{ds,on}$ measurement circuit for real-time condition and health monitoring, ensuring that lifetime targets are met.

TNO continues to increase their expertise in battery estimation algorithms based on the developments out of UC4. With this proof of concept, it has been shown that it is possible to make temperature estimations using signals from a DC charger, in an automotive battery pack. This can be used to create methods to further assess the safety of the pack and device charging strategies to increase the battery lifetime. Also, recommendations can be made regarding the communication standard between vehicles and chargers (i.e., ISO 155118) to enable the application of this technology in an industrial setting.

The feasibility of developed single-stage isolated series resonant AC/DC converter, targeting guaranteed soft-switching, was demonstrated in theory and practice by TU/e. This opens the road to more advanced modes such as V2G (with reversed power flow) and grid-forming operation. Both will become more important as the fraction of distributed sources in the grid is expected to grow compared to the classic centralized power plants.

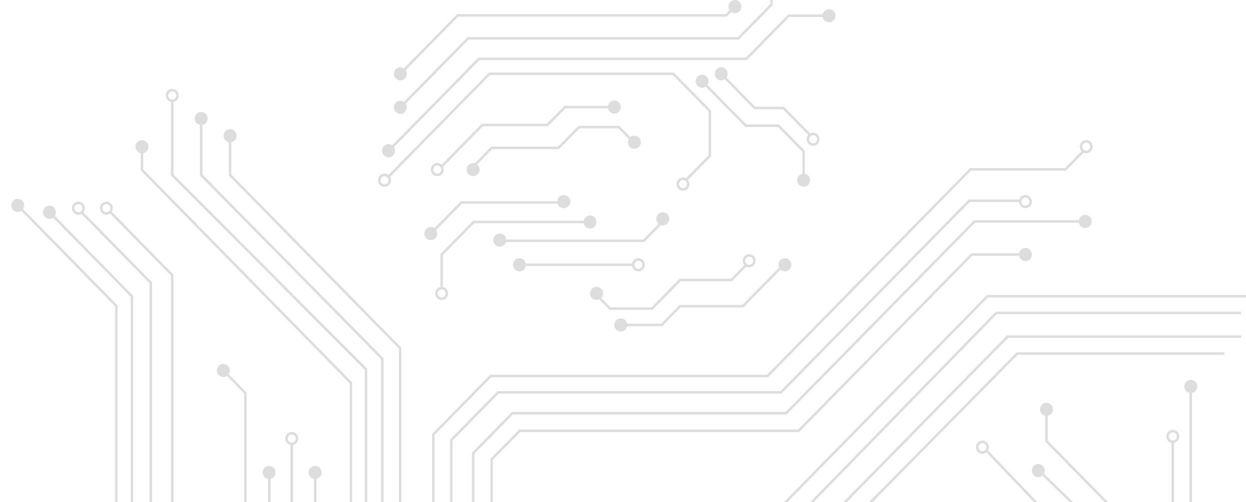
The developed AGD does not require additional signals, feedback loops, FPGAs, or a look-up table compared to other AGD systems developed and researched, while maintaining the ability to respond to changes in the system. It improves switching transient, reduces switching losses, and increases the power density of power converters. The experiment verification paves the way for future direct integration of the gate driver network into one gate driver IC.

In addition, all partners have benefited from the technical know-how accumulated in the use case. The use-case also helped the human capital development in stakeholders. The universities (TU/e, VUB, and TUDO) have been using the acquired knowledge from HiEFFICIENT in course materials and student trainings. The project itself has attracted Master and PhD students to pursue their academic and professional careers.

– Up to 98% efficiency by using optimized topologies and modulation strategies

– Design for Reliability lead to > 150,000 hours till MTBF

– Active Gate Driver Network to reduce switching losses up to 16%



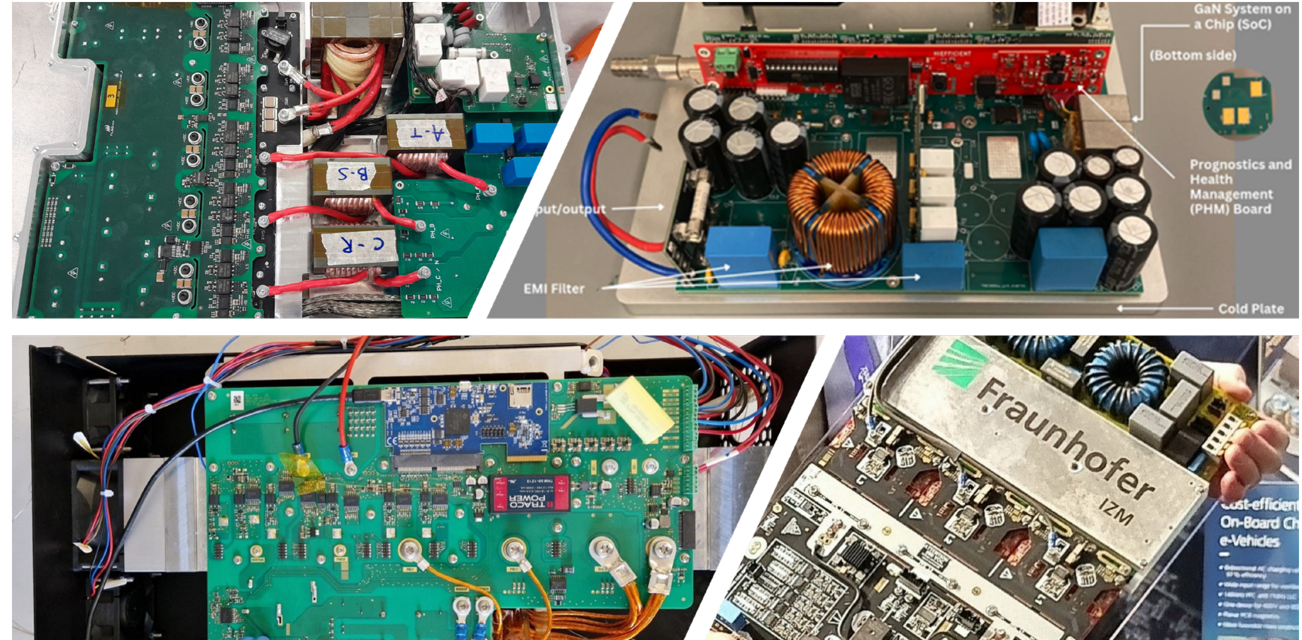
UC5

ON-BOARD CHARGERS

On-board chargers are typically restricted to slow charging due to limitations in cost, weight, and space. Generally, power electronic devices using WBG materials like GaN are rapidly advancing and are expected to significantly enhance power converters. GaN technology brings notable advantages for charging systems, being particularly competitive and mature for applications in the lower voltage range and ideal for high-frequency operations. Compared to Si devices, GaN technology results in lower losses at higher frequencies. This advantage enables the development of more compact devices with increased power density, thereby affecting the size and weight of the on-board charger. Therefore, this use case is centred on the design, optimization, and prototyping of OBCs, complemented by additional features and functions such as intelligent energy and thermal management, as well as predictive health monitoring of electronic components. Furthermore, the integration of power-factor-correction rectification stages with DC/DC converters into an OBC is demonstrated.

In total, 4 different demonstrators have been developed, which are as follows:

- ***UC5a: Smart GaN (bidirectional) on-board charger at 400 V***
- ***UC5b: Bidirectional LV off board DC charging at 48 and 120 V***
- ***UC5c1: Bidirectional OBC featuring 400 and 800 V battery voltage***
- ***UC5c2: Bidirectional OBC with integrated DC/DC converter***



UC5A

ON-BOARD CHARGERS SMART GAN ON-BOARD CHARGER 400 V

UC5a demonstrates the implementation of a GaN-based bidirectional on-board charger with 650 V switches, focusing on system integration, safety, durability, and performance optimization. The implementation of the OBC uses GaN half bridge (HB) system-on-chip (SoC) dies developed in HiEFFICIENT. Furthermore, a modular and flexible GaN devices test platform was developed, and this test-board demonstrated the deployment of these GaN SoCs, as well as with an alternative discrete GaN switch, which was employed for a parallel development on a second OBC implementation. The parallel approach with two OBC GaN systems allowed for technology comparison and demonstrating the modular flexible test board for different switches (e.g. top-side cooled discrete GaN). The OBCs consist of two stages, a PFC rectification stage and a DAB DC/DC stage. On device level, the modular flexible platform or unit allows for quick tests of the HB SoC, the discrete device and any new switch. The OBC stages are prototyped and tested separately and integrated for different modes (V2G and G2V). Efficient testing is performed in a single-phase approach, and the results presented in this section are reflecting single phase system testing, up to 2 kW per phase.

RESULTS

As part of the HiEFFICIENT project, two 400 V OBC prototypes have been developed by VUB: one based on GaN System-on-Chip (SoC) half-bridge modules developed by IMEC and AT&S in the project, and the other using commercial discrete GaN devices to demonstrate the flexibility of the OBC design and modular flexible test platform board in terms of hardware and software and for performance analysis. To ensure efficient thermal management of the GaN SoC-based OBC, a dedicated cold plate was designed via computational fluid dynamics (CFD) simulations to enhance heat transfer from active components to the cooling system. The final cold plate design features a cooling channel positioned directly beneath the GaN SoCs for efficient heat dissipation. This multi-layered configuration — comprising the printed circuit board (PCB), GaN SoCs, thermal interface material (TIM), and the cold plate — ensures effective heat transfer.

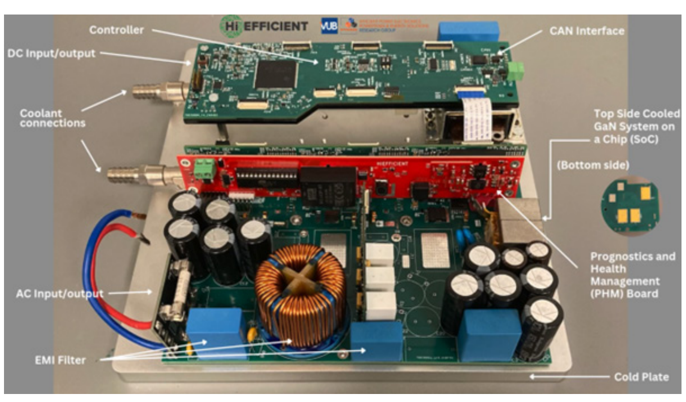


Fig. 1 Overview of the Use Case 5a demonstrator: GaN SoC-based 400 V bidirectional OBC

This UC was conducted in a collaboration of five partners:
VUB, AT&S, IMEC, SAL, TDK-DE

The contributions of each partner are described as follows:

VUB (UC LEAD): OBC design, cooling system, control deployment, prototyping and overall system integration

AT&S: embedding of the 650V GaN SoC into the printed circuit board (PCB)

IMEC: 650 V GaN System-on-Chip (SoC)

SAL: multi-physics simulation of GaN SoC chip in various embedding concepts

TDK-DE: EMC requirements and EMC design, provision of passive components

Additionally, this use case addresses the critical need for monitoring the on-state resistance ($R_{ds,on}$) of GaN semiconductor devices within the OBC. A dedicated PHM board was developed to measure the $R_{ds,on}$ of the GaN switch to estimate the remaining useful lifetime. Fig. 1 illustrates the complete two-stage GaN SoC-based OBC, highlighting key components such as the GaN SoCs, controller unit, PFC inductors, EMI filters, PHM board, custom multi-layer cooling system, and the integrated AC and DC boards.

Afterwards, the entire assembly was placed inside a custom-designed case, forming a compact, thermally efficient unit suitable for use in automotive power electronics systems (Fig. 2), such as on-board chargers for electric vehicles (EVs). The general dimensions of the OBC are 254 mm x 279 mm x 60 mm.

Testing and Evaluation of Electrical Performance

The integrated PFC and DC/DC stages, based on the discrete GaN-based variant, were tested successfully for G2V and V2G mode and Fig. 3 (a) and (b) show the PFC operation in G2V and V2G modes respectively. In Fig. 4, the waveforms are shown of the two stages integrated and tested together in V2G mode at the DC link voltage of 380 V and 2 kW power.

A fully integrated module (PFC rectifier and DC/DC) of the On-Board Charger (OBC) prototype with discrete GaN switches was tested in Vehicle-to-Grid (V2G) mode and measured with a Yokogawa WT1806E power analyser (~0.02% accuracy). In this configuration, the system achieved a measured peak efficiency of 96.7% at a DC link voltage of 340 V while delivering 1.4 kW of power to a 40 Ohm resistive load.

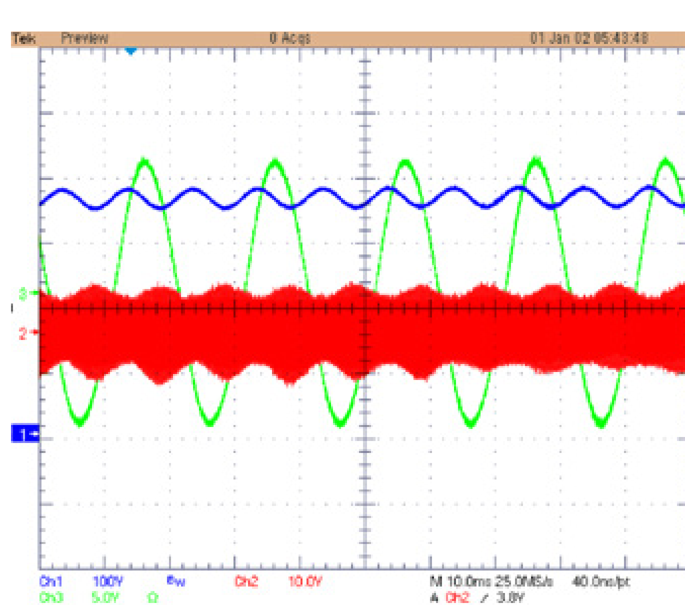
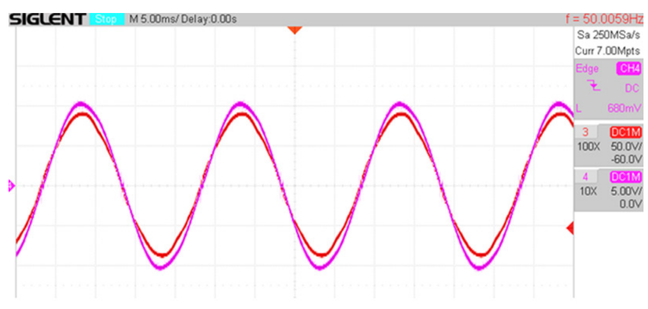


Fig. 4 Integrated OBC (PFC rectifier & DC/DC) operation in V2G mode showing single phase test with DC link at 380 Vdc and AC voltage of 230 Vrms, supplying a 40 ohm resistive load. The DC-link voltage (blue), transformer current (red), and output AC current (green) are shown

Fig. 2 The enclosure unit of OBC



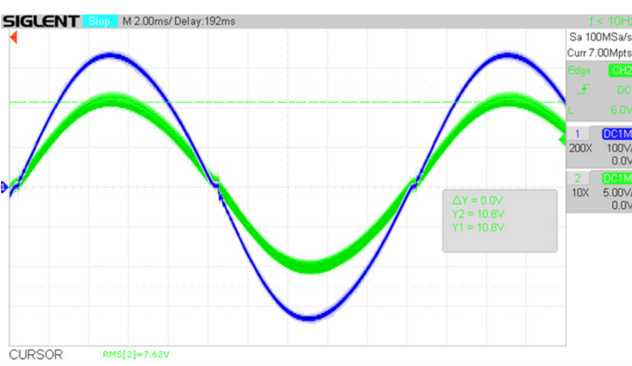
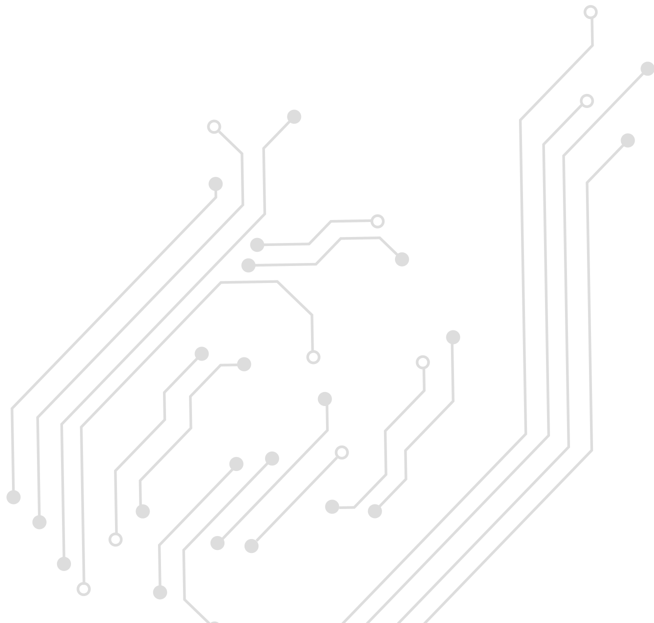


Fig. 3 PFC operation in both G2V and V2G modes single phase test: (a) G2V operation @ 200 Vdc/1 kW: grid voltage (pink) and current (red) (top), (b) V2G operation @ 230 Vrms/2 kW: AC voltage (blue) and current (green) (bottom)



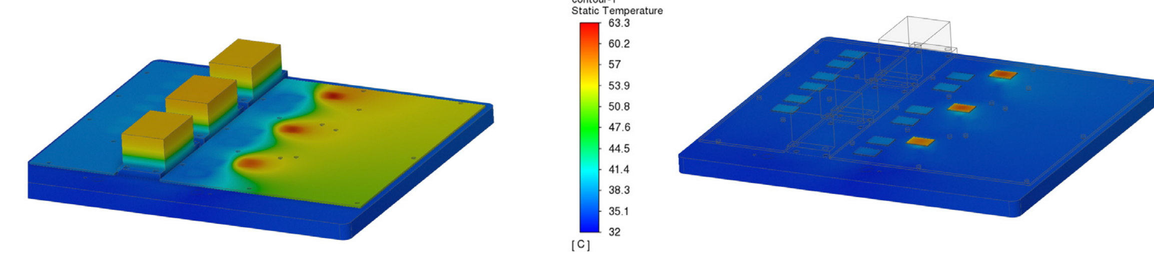


Fig. 5 CFD simulation results: (a) the OBC unit temperature distribution (left), (b) GaN SoCs temperature distribution (right)

Testing and Evaluation of Cooling Performance

CFD simulation in the design phase of the cold plate serves as a virtual model of the physical setup. By incorporating empirical test results as input parameters, it enables accurate predictions of junction temperatures as shown in Fig. 5.

Testing and Evaluation of PHM

The PHM approach for UC5a involves a semi-online measurement of the on-state resistance ($R_{ds,on}$) of the GaN SoC-based switch using a specifically designed PCB, with data subsequently transferred to the cloud for RuL estimation. The PHM board is intended to measure the $R_{ds,on}$ of the GaN switch prior to each charging cycle. To achieve this, a hardware board is configured to inject a precise 1 A current into the drain-source of the GaN switch and record the resulting drain-source voltage. This voltage measurement enables accurate $R_{ds,on}$ estimation of the switch. The $R_{ds,on}$ values are then processed in the cloud over an extended period to identify the gradual increase in $R_{ds,on}$, indicating GaN SoC degradation. A data filtering algorithm is applied alongside quadratic interpolation/regression to forecast when the GaN SoC $R_{ds,on}$ value will surpass a 20% increase from its initial value at the time of OBC commissioning. The overall methodology is shown in Fig. 6.

For proof-of-concept validation, $R_{ds,on}$ was measured continuously at 5-second intervals rather than using a single acquisition (as planned for final use). Additionally, the temperature of the GaN SoC was increased to verify if the PHM board could track $R_{ds,on}$ changes in response to temperature rise. The temperature increase was monitored by measuring the voltage on the PTC of the GaN. The PHM board transmitted the recorded $R_{ds,on}$ values to a local PC via a CAN-serial converter, where the data was logged and visualized. The resulting dataset from the validation test is presented in Fig. 7.

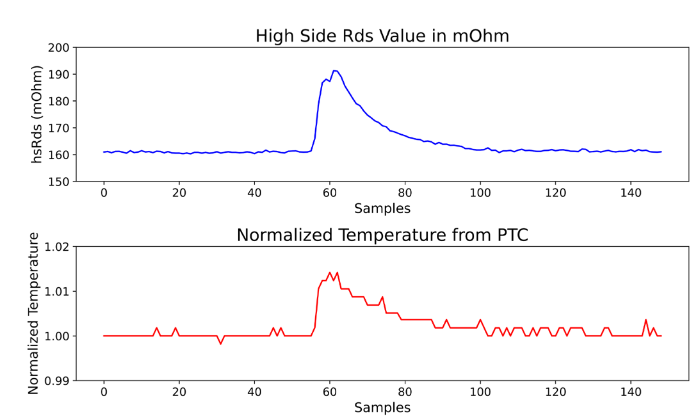


Fig. 7 Validation of $R_{ds,on}$ measurement by the PHM board, demonstrating accurate tracking with temperature increase

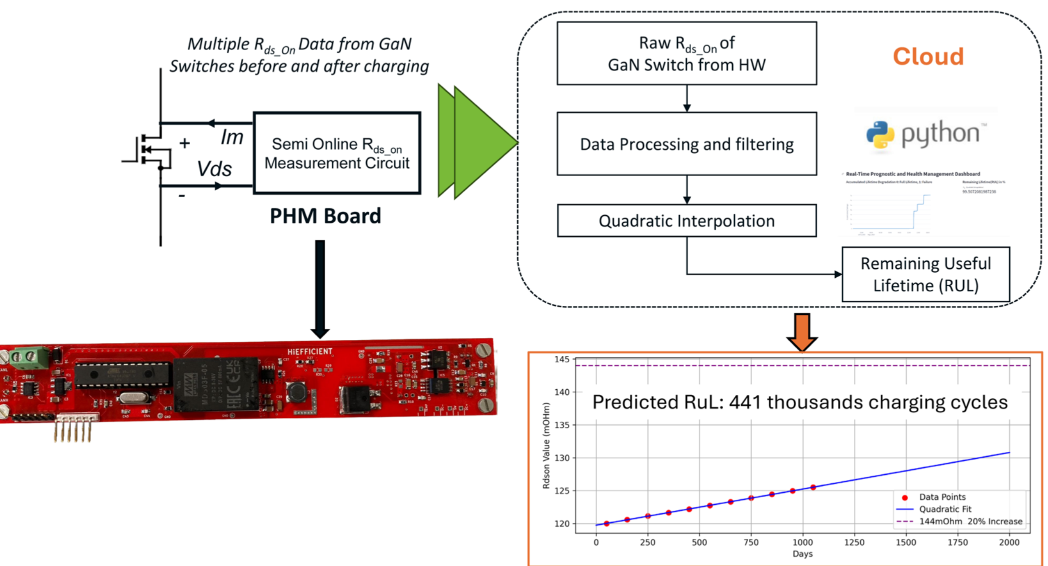
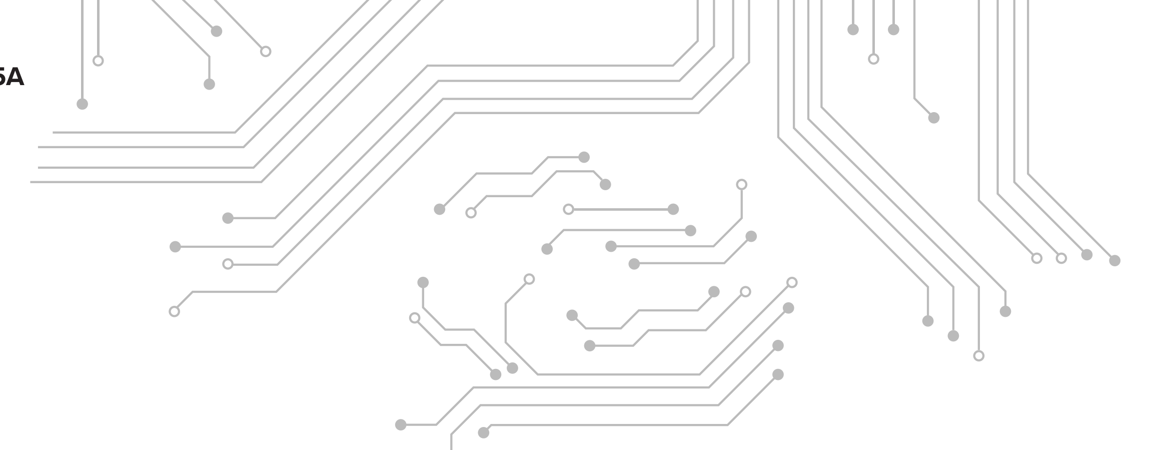


Fig. 6 Overview of the PHM methodology for UC5a on-board charger



IMPACT OF UC5A

UC5a has contributed to the advancement of next generation electric vehicles' GaN-based on-board chargers by addressing integration and hardware testing challenges, power density and optimizing key aspects like thermal management, and efficiency for next-generation wide-bandgap semiconductors. Through the HiEFFICIENT project, two bidirectional charging prototypes — one using GaN System-on-Chip modules have been designed, developed and demonstrated and another with commercial GaN devices — allowing insights into packaging, bidirectional capability and control, and real-time on-state resistance ($R_{ds,on}$) monitoring which was implemented for reliability assessment.

In this use case, an innovative power electronics optimization approach was introduced, incorporating Design for Reliability (DfR) to enhance system efficiency, reduce size, and extend the lifespan for both the PFC rectification and isolated DC/DC stages. During testing of the UC5a prototypes, a maximum efficiency of 97% was measured. The different prototypes' modules were efficiently tested via a flexible modular electronics platform developed in this use case. Finally, a flexible in-situ $R_{ds,on}$ measurement circuit for real-time condition and health monitoring was developed and deployed in this system.

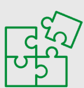
AT&S has contributed with embedding and packaging of the SoCs developed by IMEC. The design of the package for the SoC was developed and realized in close cooperation with VUB, who later implemented it in the OBC prototype.

IMEC has contributed to the realization of the SoCs, with designs, various topologies (variants), and chip IOs. The functionality of the SoCs was also tested by IMEC, who delivered different batches of diced wafers (1st and 2nd learning cycles in the project). Interposer boards (dedicated small PCBs), to which a bare die or packaged SoC can be wire-bonded and then connected to a larger board for functionality testing were also provided.

TDK-DE has designed the OBC's EMC filter concept for AC and DC ports based on simulation results and provided the components for implementation. While meeting EMC requirements of conducted emissions, the design is optimized for compact design and low losses in the passives.

VUB closely collaborated with the partners on the design specs for the SoC and its interfaces. Then, a full multiphysics (electrical-thermal) design framework for OBC systems with different switches and their PHM board was proposed, designed, prototyped, tested, and evaluated. In this use case, two bidirectional OBC systems, one based on the HiEFFICIENT SoCs and a second one with off the shelf discrete GaN devices were evaluated.

UC5a Achievements



– Compact automotive reference design with 2.6 kW/l power density, upscalable in power

– 97% efficiency measured, thanks to high-frequency GaN PFC and DAB stages

– Design for reliability ensuring an operational lifetime of more than 11 years
– $R_{ds,on}$ based RUL estimation via smart edge-cloud framework

UC5B

ON-BOARD CHARGERS BIDIRECTIONAL LV OFF-BOARD DC CHARGING AT 48 AND 120V

In UC5b, the partners developed a modular, bidirectional low-voltage off-board DC charger solution (48 V and 120 V; maximum power 7 kW) along with an on-board DC/DC 12-48/120 V converter for a low-voltage battery electric vehicle, which is equipped with solar panels for daytime charging, but no on-board charger.

The basic setup of the off-board charging system is illustrated in Fig. 1 and includes two main components: an AC charger and a DC charger. These use standardized charging interfaces to connect both the AC and DC chargers, as well as the DC charger to the vehicle, facilitating independent use of each component. The developed AC charger, a so-called wall box, can also serve all electric vehicles with on-board chargers for low power, e.g., home charging. And the DC charger is designed to be very compact and could be taken with the light electric vehicle for charging at any available AC connection.

Further, the on-board DC/DC converter converts the voltage of the solar panels to 100 V and 48 V while also performing the 100/48-12 V DC/DC converting stage. The multifunctional DC/DC converter unit also integrates the battery management system (BMS) and operates in a CAN based network.

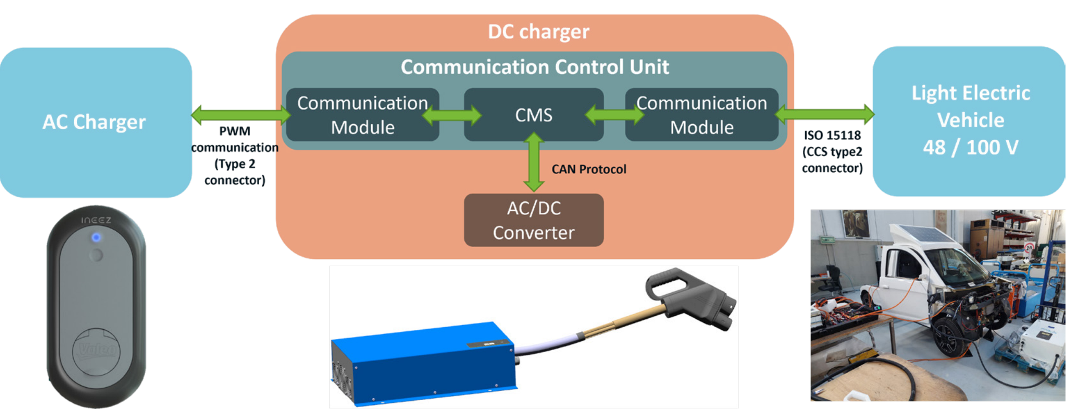


Fig. 1 Overview on UC5b

This UC was conducted in a collaboration of four partners:
VSCM, AVL-SFR, HELIOX, I-FEVS

The contributions of each partner are described as follows:

VSCM (UC LEAD): developed the AC grid integration

AVL-SFR: developed a GaN based AC/DC converter

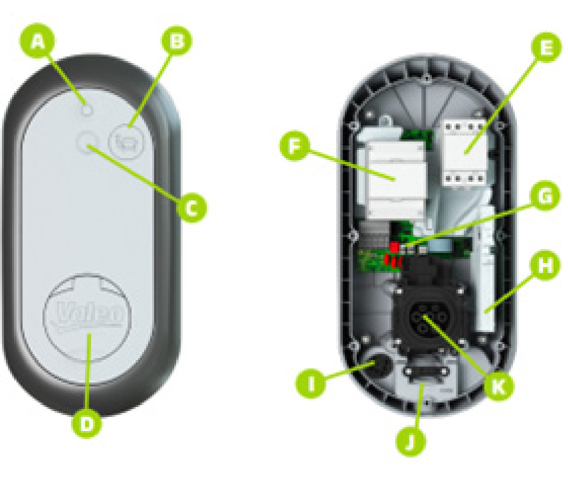
HELIOX: worked on the Communication Control Unit

I-FEVS: focused on the on-board DC/DC 12-48/120 V converter as well as preparing the LEV for DC low-voltage charging; additionally developed an integrated DC charger.

RESULTS

AC charger

The demonstrator developed by VSCM is a 7 kW charger at 220 V and is OCPP 1.6j compliant (Fig. 2). The charger has further GSM 4G LTE, LAN, and WIFI connectivity to maximize user experience. The demonstrator was developed according to embedded automotive standards. The demonstrator was thoroughly and successfully tested to prove its safety and robustness during life of the product (cybersecurity, IP55, IK10, RCM).



- A. **LED** / LED
- B. **Lecteur RFID** / RFID reader
- C. **Zone tactile** /Touch sensor
- D. **Clapet** / Flap
- E. **Contacteur** / Contactor
- F. **Compteur MID (option)** /MID meter (optional)
- G. **Borniers de raccordement** / Connection terminals
- H. **Port RJ45 _ emplacement carte SIM** / RJ45 _ Sim card slot
- I. **Entrée câbles Bobine MX _ Linky _ RJ45 _ compteur dédié** / MX coil _ RJ45 _ submeter input
- J. **Entrée câble de puissance** / Power cable inlet
- K. **Prise** / Socket

Fig. 2 AC charger overview and available features Overview on UC5b

DC charger

The DC charger consists of an AC/DC converter and a communication and control unit, to control the power electronics as well as does the communication with the outside world, the AC charger and the vehicle (Fig.3 and Fig.4). The power electronics charger created by AVL-SFR includes a PFC stage for power factor correction and a DC/DC converter for the required isolation, output voltage, and current. The digital PFC uses a bridgeless totem pole topology with GaN switches at 140 kHz, while the DC/DC stage is a CLLC converter using GaN technology at 400-650 kHz. All control tasks are managed by a microcontroller, and a CAN interface connects to a higher-level control unit.

Tests of the PFC show it operating up to an input voltage of 230 Vrms and boosting to a DC-Link voltage of 450 V. The CLLC converter was tested with an input of 450 V and an output range from 36 V to 60 V but could only achieve 1.5 kW due to thermal constraints of the GaN switches. Thermal measurements showed a too high resistance from the device junction through the PCB and cooler, differing from the expected values based on the available datasheets. Hence, for all further tests the output power was consequently limited to ~1.5 kW not exceeding the thermal limitations of the power electronics under test. Tests used a 230 Vrms AC input and a 48 V output setpoint, showing the expected results, as well being compliant with EN61000-3-2 (grid current harmonics within limits for currents up to 16 A and power over 75 W). However, due to the thermal issues and still ongoing investigations, a complete integration could not be completed.

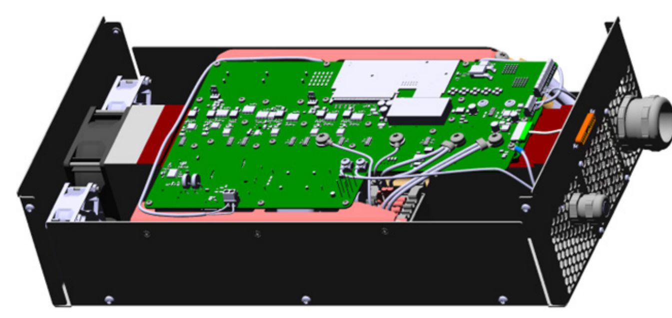


Fig. 3 Rendering of DC charger

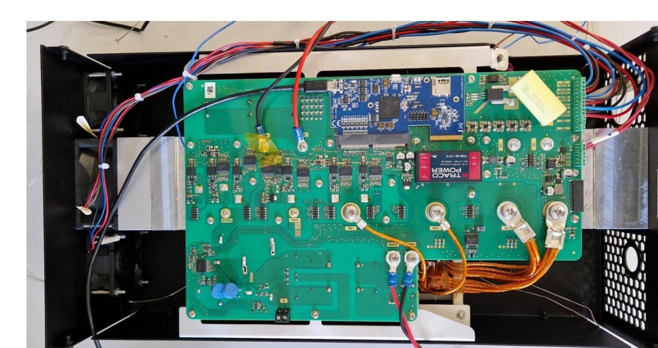


Fig. 4 DC charger integrated in housing

Light Electric Vehicle

The light electric vehicle to be charged was developed by I-FEVS, using a Valeo 48 / 100 V based powertrain. In the course of the project, I-FEVS worked on implementing a bidirectional DC-DC converter operating at 48 V and 100 V, being in line with voltages adopted in its pick-up and van, having integrated solar panels and related power and concertation electronics.

The on-board DC/DC converter converts both the voltage of the solar panel to 100 V and 48 V respectively, while also performing the 100 / 48 - 12 V DC/DC converting stage. The multifunctional DC/DC converter unit integrates the battery management system (BMS) and operates in a CAN based network. The converter also covers the battery balancing. I-FEVS has patented the solution to optimize the energy flow from solar panels towards the battery pack for balancing purposes.

Parallel to the developments above, I-FEVS developed a separate bidirectional single phase DC charger for their vehicles at 48 V and 100 V without a dedicated interface to the AC charger (Fig. 5). Important functional parameters are as follows:

- Input voltage single phase (min, max): 197 Vac – 254 Vac
- Output voltage (min..max): 48 V..250 V
- Output current max: 60 A
- Output Power: 7 kW (limited by the output current)
- Output Power @100 V (M1 vehicle): 6 kW
- Output Power @48 V (N1 vehicle): 2.88 kW
- Communication / connector standard: CCS2
- EMC Class B according to IEC 61851-21-2

On the vehicle side I-FEVS implemented a dedicated socket which is placed aside on frontal fender. A customized circuit board was implemented to connect the charging station with the vehicle itself. The E/E architecture of the vehicle developed by I-FEVS is based on CAN-bus protocol communication that requires a dedicated connector. The battery-packs are interfaced with the charging system via CAN-bus protocol referred to the related regulation of CAN2.0B and J1939.

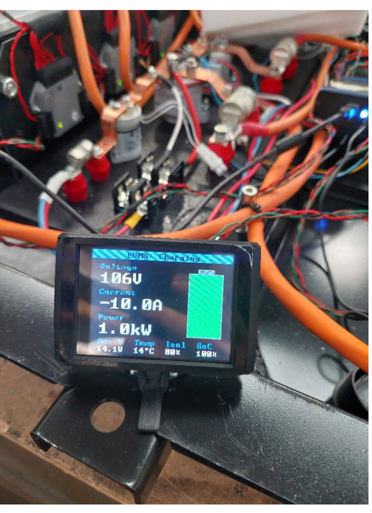


Fig. 5 DC charger in operation

IMPACT OF THE UC5B

The use case successfully demonstrated several technologies beneficial for future developments and at the end for customer usage.

- Valeo developed an AC Charging Station with up to 22 kW charging power, having a focus on simplicity and robustness. being brought as product to the market soon.
- AVL-SFR demonstrated the applicability of GaN devices in a low-voltage DC charger application, having a 140 kHz PFC stage compared to 100 kHz state of the art. An iso stage in CLLC topology with up to 650 kHz switching frequency and digital control software was realized. Thereby latest GaN switches were used to reach an 98% efficiency target. An on-board Rogowski current measurement was implemented and tested due to the lack of available solutions in the market for these switching frequencies. A follow up project with an automotive OEM has already started based on the know-how collected in this use case.
- I-FEVS demonstrated that recharging low-voltage vehicle (48 V, 120 V) is possible with the same services enabled for high-voltage electrical vehicle. Moreover, when the vehicle is plugged in, you can use the energy stored in the battery for your power needs. The developed DC/DC converter demonstrator applies a novel patented technology allowing automatic dynamic voltage regulation for battery charging and discharging.

UC5b Achievements

– Highly compact AC charger design

– 98% efficiency target with 650 kHz iso stage switching frequency

UC5C1

ON-BOARD CHARGERS BIDIRECTIONAL OBC 400-800V

Charging on public AC grids is essential for the success of e-mobility. In UC5c, Fraunhofer IZM has made significant achievements by integrating the latest advancements in power electronics for the next generation of on-board chargers. The first UC5c demonstrator is dedicated to the development of an On-Board Charger (OBC), allowing to charge batteries at 400 V and 800 V standard, thanks to a reconfiguration of the output of the battery charger topology. The demonstrator works in three-phase and single-phase configuration with a wide output power range, going up to 22 kW in 3-phase configuration. Thereby a focus was on a most compact design, enabling bidirectional charging, highest efficiency, and easy manufacturability to minimize production costs by facilitating innovative PCB and packaging solutions for an automated production.

RESULTS

Fraunhofer IZM has advanced the design of electric car on-board chargers (OBCs) significantly. To achieve this, the two main components of a charger had to be rethought.

Every OBC includes a crucial component known as the power factor correction (PFC). The PFC serves as the interface with the public grid, ensuring that the incoming alternating current is shaped into a stable sine wave, typically at 50 or 60 Hz, depending on the local grid. This process relies on chokes, which are bulky and expensive components in traditional OBC designs.

Fraunhofer IZM has developed a flat PFC inductor designed as a circuit board with four magnetically coupled coils on a shared ferrite core. This new PFC choke is not only significantly smaller but can also be manufactured by machines rather than by hand. Although the planar design results in lower inductance, this is not an issue for PFCs equipped with Silicon Carbide (SiC) switches that operate at 140 kHz. The design makes it possible to replace all electrolytic capacitors with much more reliable and durable filament capacitors with an order of magnitude smaller capacity.

The second crucial component is the transformer. The primary function of this component is to ensure that the car battery remains galvanically isolated from the public grid, as parasitic leakage currents to the earth generated by the OBC could lead to and potentially disrupting or even disable the common protection system of the grid installation, so called residual current circuit-breaker (RCD). To solve the problem, the vehicle is isolated from the mains using a transformer integrated into the OBC. Fraunhofer IZM has developed a resonant high-frequency transformer which leverages cutting-edge wide-bandgap semiconductors made from gallium nitride (GaN). These new GaN switches enable the resonant transformer to operate at clock frequencies of 1 MHz and above. Thanks to the innovative technology, this usually bulky transformer could also be manufactured as a very compact planar PCB based assembly.

Using standardized and proven PCB technology, the OBC can be produced fully automatically in assembly lines, which saves manual work and manufacturing costs. In addition, the amount of copper required for the magnetic components has been drastically reduced. The combination of these and other components enables a future-oriented OBC with excellent properties:

- Space requirement of only 3 liters
- Low production costs because it can be manufactured by machine
- Compatible with 1-phase and 3-phase AC grids of different voltages up to 22 kW
- High efficiency of 97%
- The same electronics for 400 and 800 V batteries
- Bidirectional charging to use car battery as local energy storage

This UC was conducted in a collaboration of two partners:
FHG, IFAG

The contributions of each partner are described as follows:

FHG (UC LEAD): design and development of on-board charger

IFAG: development of a 3-level GaN module

IMPACT OF UC5C1

Drivers used to high-power charging (HPC) can expect their electric cars to be charged in about 15 to 30 minutes. This rapid charging is made possible by the immense power of up to 350 kW these chargers provide. The power is supplied in DC, which is ideal for electric vehicle batteries, allowing for direct charging without the need for an on-board charger.

In contrast, AC chargers are far more common. These include standard household sockets, which offer up to 3 kW from a single phase of AC current. Three-phase AC current from public EV charging point or wallboxes can provide up to 22 kW, enabling many car batteries to be fully charged in around four hours. However, many current electric vehicles are designed to accept a maximum of 11 kW due to limitations in their on-board chargers (OBCs). These traditional OBCs are typically a collection of multiple separate components, including large inductors that are often manually manufactured and assembled, taking up significant space in the vehicle. While some car manufacturers offer an upgrade from 11 to 22 kW, either by adding a second OBC or using a larger module, both come with increased costs and space requirements. Moreover, most OBCs operate unidirectionally, meaning they only charge the car battery and cannot send stored energy back to the grid or allow parked EVs to serve as buffers for home solar power systems. As a result, the vision of electric vehicles supporting the green energy transition as a distributed energy storage network remains unfulfilled with current technology.

Fraunhofer IZM has successfully integrated some of the most innovative concepts in power electronics, leading to a new generation of on-board chargers. With double the performance in half the size, bidirectional capabilities, and efficient machine manufacturing, this on-board charger serves as an economical fast lane of the future.

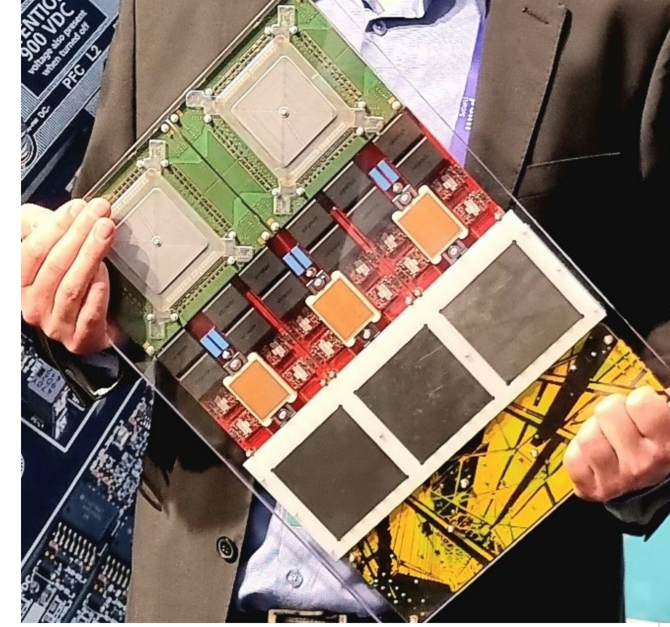


Fig. 1 UC5c1 on-board charger without housing

UC5c OBC 400-800 V Achievements

- 22 kW OBC in 3 liter, i.e. 7 kW/l
- very wide 75-480 Vac input / 240-870 Vdc output

- Efficiency 97% with 140 kHz PFC and 1 MHz LLC operation

UC5C2

ON-BOARD CHARGERS BIDIRECTIONAL OBC+DC/DC

Second UC5c demonstrator focuses on developing an integrated EV On-Board Charger (OBC+DC/DC) that incorporates a high-voltage to low-voltage DC/DC converter (HV to LV DC/DC). This essential component in all-electric vehicles supplies power to most auxiliary loads on-board, traditionally implemented as a separate device. To reduce the component count, minimize volume and weight, and enhance system efficiency, the integrated OBC and DC/DC converter share a common HFT (High-Frequency Transformer). This shared component provides galvanic isolation and further cost reductions.

The OBC enables battery charging at 400 V standard, drawing a maximum power of 22 kW from the grid and supporting bidirectional power flow. This bidirectional capability allows for vehicle-to-grid (V2G) operation, contributing to grid stability by integrating the electric vehicle as both a load and a potential energy source. To enhance system performance and longevity, the OBC incorporates additional features as intelligent energy and thermal management optimizing energy usage and prevents overheating and also Predictive Health Monitoring (PHM) by tracking the health of electronic components, enabling proactive maintenance and reducing downtimes.

These features collectively contribute to reducing running costs and extending the overall system's lifespan. Moreover, PHM improves serviceability and facilitates easier maintenance of the OBC.

RESULTS

FLAG-MS, as the developer of this UC demonstrator, focused on designing, optimizing, and prototyping a bidirectional On-Board Charger (OBC+DC/DC). The OBC incorporates 650 V GaN devices in the converter interfacing with the 400 V battery, while 1200 V SiC MOSFETs are utilized in the section interfacing with the grid. Additionally, 100 V GaN transistors are employed for the low-voltage DC/DC converter.

The aim was to develop an OBC with a power rating of 22 kW, including a 3 kW DC/DC converter. All necessary components were mechanically integrated into an aluminum case with a total volume of 13.7 liters, incorporating a cooling system to ensure efficient operation.

The PFC and primary DC/DC converters share a common PCB, an IMS (Insulated Metal Substrate) for enhanced cooling. These converters were tested together in G2V mode at various voltage and current levels on the HV battery side. While full performance was not achieved due to thermal management limitations (forced air cooling instead of liquid cooling), the tests provided valuable insights. Test results indicate a peak efficiency of approximately 96% at 11 kW, considering the combined efficiency of the PFC, grid emulator, pre-charge stage, and input grid filter (therefore without the CLLC).

The estimated efficiency of each individual stage is around 98%. The CLLC alone showed an efficiency greater than 97% during a test with a power flow of 12.85 kW from primary to secondary converter. The complete G2V operation was tested up to 7.5 kW with an efficiency of around 93.9%, considering also the grid emulator. Thus, the estimated efficiency (without the grid emulator) is higher than the previous value.

The complete OBC+DC/DC system and its logical scheme are illustrated in Fig. 1.

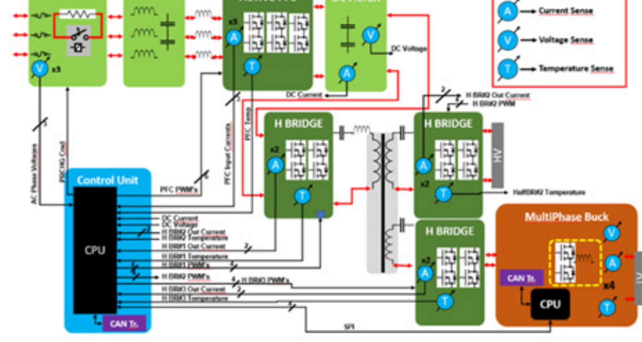
Furthermore, UNIPisa developed a PHM algorithm to enhance converter operation. For the development and evaluation, electrothermal model estimations and simulations of the OBC+DC/DC have been used. The final hardware is still undergoing testing.

This UC was conducted in a collaboration of two partners:
FLAG-MS, UNIPISA

The contributions of each partner are described as follows:

FLAGS-MS (UC LEAD): developed and prototyped the integrated EV On-Board Charger (OBC+DC/DC) and all necessary components

UNIPISA: is implementing and testing the PHM algorithm on an MCU board for the OBC



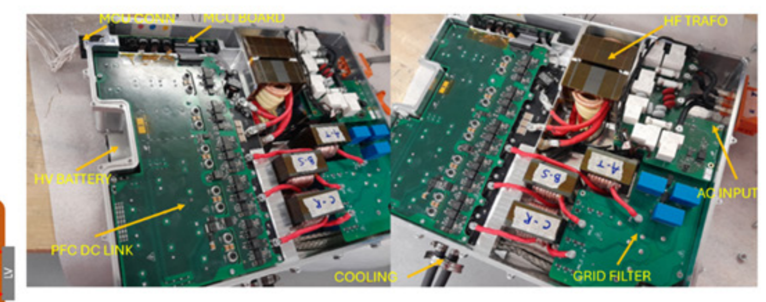


Fig. 1 OBC+DC/DC and relative logical scheme

IMPACT OF UC5C2

The integrated EV On-Board Charger (OBC+DC/DC) incorporates several innovative features, resulting in a high-performance and compact solution. By employing WBG devices, the converter achieves reduced filter requirements, contributing to its overall size and weight. The integrated DC/DC converter further enhances system efficiency and reduces complexity.

The experience gained during the project led to the possibility of integrating the DC/DC converter for the on-board auxiliary elements within the OBC itself. This type of OBC setup can replace parts of the existing on-board power electronics and increase the power density of the system.

Additional PHM features estimating the junction temperature, enable an increase in reliability and estimate the expected life time of the electronics.

UC5c OBC +DC/DC Achievements

- OBC + DC/DC integrated

- Intelligent thermal and energy management to prevent overheating
- PHM features to extent lifetime

UC6

MODULAR DC/DC CONVERTER FOR LOW-POWER PV SYSTEMS

The initial use case focus was on GaN-based DC/DC converters designed for solar electric vehicles, aiming to significantly boost converter efficiency to maximize the overall solar yield and therefore the range of the vehicle by optimizing the performance of these converters. However, the progress of UC6 was severely impacted by the exit of the UC lead, Lightyear, due to bankruptcy. Therefore, at quite a late stage in the project, the scope was redefined, and the technological ambition adjusted to the overtaking partner's interest and capabilities – the efforts of the consortium shifted to developing a low-power, modular DC/DC converter suitable for PV applications as these relate to the automotive sector. From a scientific perspective, UC6 retained the focus on the comparison of the newly developed GaN devices by IFAT (100 V SiP) and IMEC (100 V SoC) as these were specified at the initial phase of the project. The objective was to evaluate their reliability in testing and compare them in the context of the design, development, and performance of the DC/DC converter.

RESULTS

The project successfully developed and delivered engineering samples of the relevant GaN devices towards the UC. A GaN-based DC/DC converter utilizing Infineon devices was designed, prototyped, tested, and evaluated for performance.

The design of the converter was done according to the specifications defined with the partners. A brief recap of the key points is as follows:

- Input voltage of the converter is in the range of 20 to 40 V and output voltage is set to be 48 V
- The nominal power is specified at 250 W
- The converter was built around the 100 V CoolGaN integrated power supply (IPS) package provided by Infineon, which embeds a GaN half-bridge, gate driver, and decoupling capacitors in a small footprint (6x9 mm) laminate package, featuring around 3 mΩ on-state resistance.
- Small heatsinks with natural convection have been used for the cooling of the power semiconductors.
- The auxiliary power supply circuit taps directly from the input voltage through a buck regulator stage.
- A planar coupled inductor was designed to offer output current ripple cancellation and better utilization of the magnetic core. Moreover, the PCB-embedded coils and planar design enabled much higher power density compared to discrete inductors.

This UC was conducted in a collaboration of eight partners:
TU/E, FHG, IFAT, IMEC, NANO, STUBA, TUC, TNO

The contributions of each partner are described as follows:

TU/E (UC LEAD): specification, DC/DC converter design and implementation, performance and efficiency validation

FHG: packaging 100 V SoC half-bridge devices

IFAT: 100 V GaN SiP half-bridges with integrated driver; application development support

IMEC: 100 V SoC half-bridge devices; application development support

NANO: reliability of 100 V GaN SoC & SiP devices

STUBA: reliability and characterization 100 V GaN SoC & SiP devices

TUC: thermo-electro-mechanical modeling and reliability assessments of integrated GaN

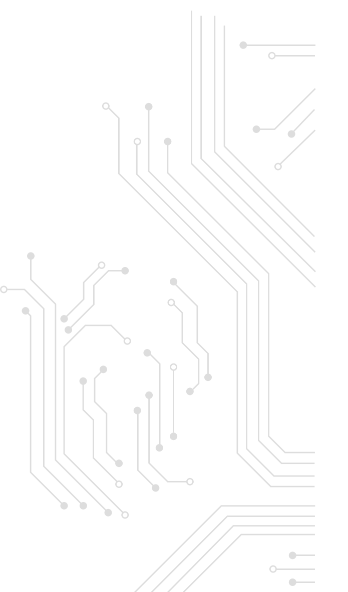
TNO: DC/DC converter performance testing

The GaN prototype demonstrated efficiency comparable to that of a silicon-based version used as a reference, but with the advantage of a higher switching frequency, which allows for increased power density. However, in both converter prototypes, the inductor power loss plays a dominant role compared to semiconductor losses, emerging as the main limitation to efficiency in this topology. When auxiliary power consumption is equalized, the GaN prototype outperforms the silicon version, highlighting its potential for superior performance in power conversion applications.

IMPACT OF UC6

The design showcased significant application benefits, particularly in boosting converter efficiency, which is essential for maximizing the yearly solar yield and extending the range of solar electric vehicles. By focusing on minimizing the converter size and maximizing power density through component integration via System-on-Chip (SoC) technology, the design effectively addresses the need for compact and efficient energy conversion solutions.

This innovation is particularly relevant for various market segments, including solar vehicle manufacturers who require advanced power management systems to enhance the performance of their vehicles. Additionally, the technology can be applied to low-power solar energy interfacing across multiple domains, such as automotive applications and DC microgrids, making it a versatile solution in the growing field of renewable energy integration.



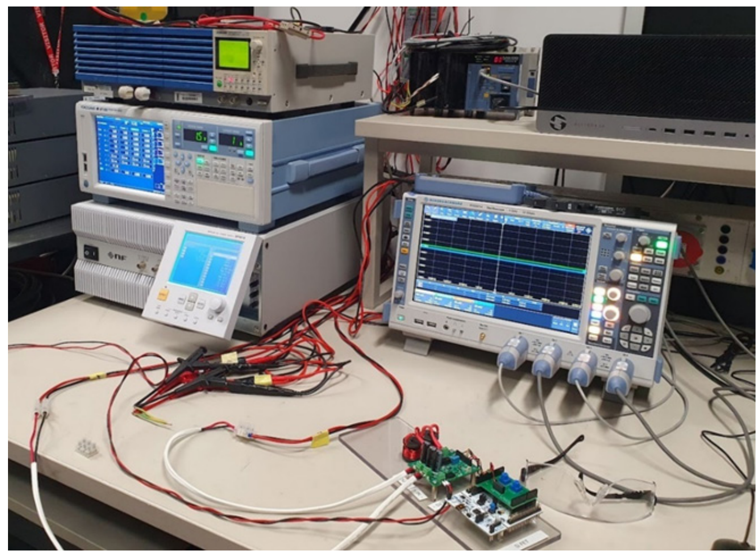


Fig. 1 Efficiency measurement setup at TNO

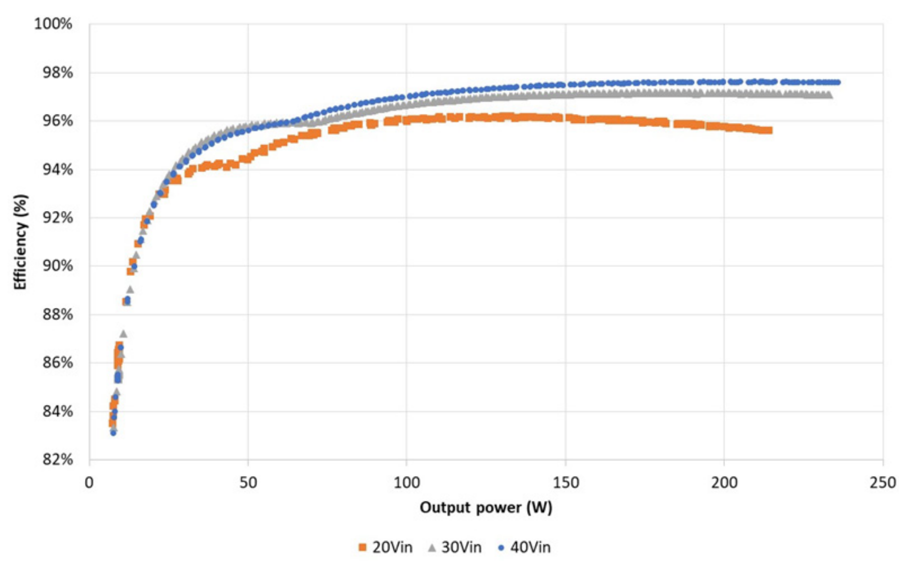


Fig. 2 Measured efficiency curves vs output power for the GaN prototype (fs=500 kHz)

UC6 Achievements

– 100 V SiP devices operated at 500 kHz switching frequency for most compact DC/DC converter design

– Low voltage DC/DC converter with 98% peak efficiency based on 100 V GaN SiP devices

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	Kompetenzzentrum – Das Virtuelle Fahrzeug, Forschungsgesellschaft mbH	ViF	Inffeldgasse 21A 8010 Graz	AT
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	TDK Electronics AG	TDK-DE	Rosenheimer Straße 141E, 81671 München	DE
	Atlas Technologies B.V. (Lightyear)	LY	went bankrupt	NL
	AVL SET GmbH	AVL-SET	Spinnerei 8 88239 Wangen	DE
	FLAG-MS	FLAG	Via Luigi Einaudi 29, 10024 Moncalieri	IT
	Ideas & Motion SRL	I&M	Via Moglia 19 12062 Cherasco	IT
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	Silicon Austria Labs	SAL	Sandgasse 34 8010 Graz	AT
	TU Chemnitz	TUC	Reichenhainer Straße 70 09126 Chemnitz	DE
	Politecnico di Torino	POLITO	Corso Duca Degli Abruzzi 24 10129 Torino	IT
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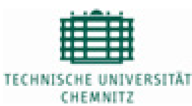
	AVL Arastirma ve Muhendislik Sanayi ve Ticaret Limited Sirketi	AVLTR	Akpınar Mahallesi Tuna Caddesi Ballıca Sokak No: 1 34885 Sancaktepe/Istanbul	TR



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